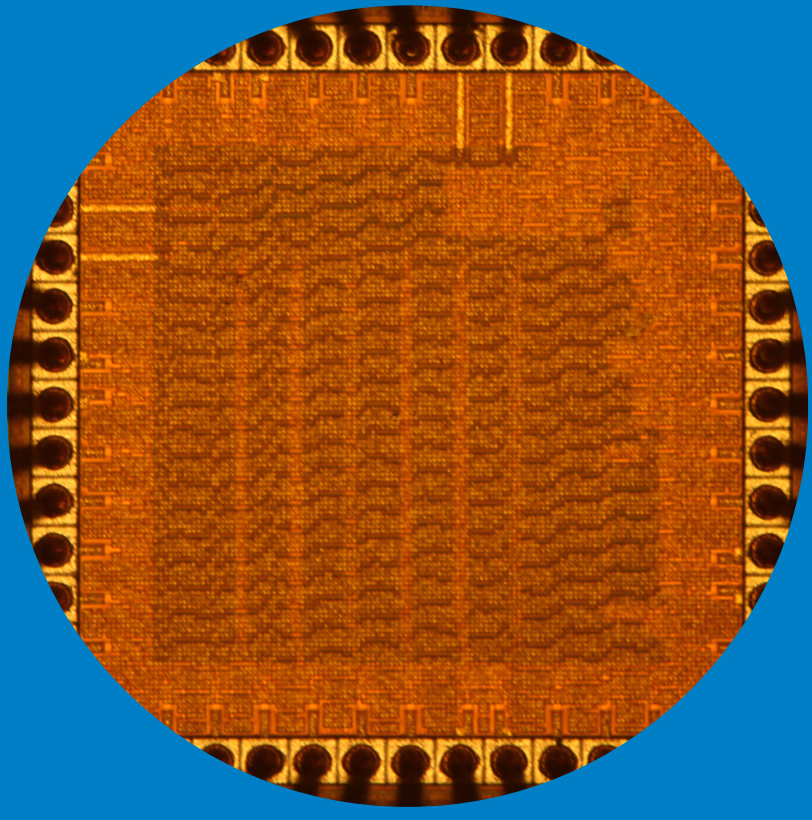
Department of Micro- and Nanosciences

Integrated DC-DC Converters for Adaptive Ultra-Low-Energy Processors

Matthew Turnquist



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Integrated DC-DC Converters for Adaptive Ultra-Low-Energy Processors

Matthew Turnquist

A doctoral dissertation completed for the degree of Doctor of Science (Technology) to be defended, with the permission of the Aalto University School of Electrical Engineering, at a public examination held at the lecture hall S1 of the school on 21 January 2016 at 12:00.

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Abstract

There is an emerging class of energy-constrained adaptive processors that operate primarily at near-threshold (NT) voltages. Operating at NT significantly reduces energy consumption but avoids the large variance and performance penalties of sub-threshold. NT processors are useful for sensor-based platforms within ultra-portable electronics that require minimum energy consumption. Typically, the NT voltages are supplied by a DC-DC converter. Energy consumption of the DC-DC converter/processor system is proportional to the DC-DC's conversion efficiency. Thus, supplying the NT voltage with high efficiency is essential in realizing ultra-low-energy consumption. High efficiency over an increasingly large power range (due to large differences in sleep and active power levels) also require careful consideration. Besides the challenges in efficiency, the DC-DC converter should be fully integrated to meet the increasingly small form factor requirements of modern ultra-portable electronics.

Research work presented in this thesis addresses the previous challenges by introducing new NT DC-DC converters, new techniques for reducing the increasingly dominant DC-DC control circuitry power losses, and new DC-DC/processor co-design methodologies. There are three main focus areas within the thesis: SC DC-DC converters, adaptive processors, and DC-DC converter/adaptive processor systems. The thesis gives the necessary background of DC-DC converters and adaptive processors. The research work is demonstrated with five integrated circuit (IC) implementations and ten publications.

Three of the IC implementations are fully integrated SC DC-DC converters. A step-down Dickson topology in 28 nm CMOS is first presented. An improved Dickson converter and a self-oscillating converter are then presented. Both of these converters are built in 28 nm UTBB FD-SOI, and both take advantage of the strong impact of back-gate biasing in order to improve efficiency. Practical design considerations of the converter's input voltage are shown with a prototype Li-ion battery. All three of the implemented DC-DC converters are measured with adaptive (processor) loads.

The final two IC implementations are adaptive processors. Both of the processors are built in 65 nm CMOS. The processors use an adaptive scheme called timing-error detection (TED) to ensure reliability at NT voltages. One of the processors is the first-known TED processor

Keywords Switched-capacitor DC-DC converter, power management, minimum energy point, sub-threshold, weak inversion, MEP, UTBB FD-SOI, ultra-low-voltage, timing-error detection, near-threshold, ultra-low-power

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Preface

The work in this dissertation was conducted at the Department of Micro- and Nanosciences (Electronic Circuit Design Group) at Aalto University. The work was supported through a number of projects. Thanks to the Academy of Finland (projects: 140340, 13139458, 270585, 124029), the Finnish Graduate School of Electronics Telecommunications and Automation (GETA), the Technology Industries of Finland Centennial Foundation (project MepMic), the EU grant 621439 (Almarvi), and Tekes 2948/31/2011. Thanks also to the Ahlström Säätiö for their financial support.

A warm thanks to Professor Alex Fish and Professor Eby G. Friedman for reviewing this thesis. Thanks to Professor Joseph Shor for agreeing to be the opponent.

Thanks to the Department of Micro- and Nanosciences for giving me the opportunity to do research in the microelectronics field. Thanks to Professor Kari Halonen for welcoming me into the ECDL. Thanks especially to my supervisor Adjunct Professor Lauri Koskinen. You gave me a chance on your team. You kept me on target and helped me come back to reality many times. Thanks for letting me move into a subject that interested me more. Most importantly of all, you introduced me to Eläkeläiset during our tapeouts. But really, my work would not have been possible without you. Professor Jussi Ryynänen – thanks for the feedback. And yes Jussi, I think very positive now. Thanks to Jani Mäkipää and Arto Rantala (VTT) for the help and great discussions. Thanks to TRC for welcoming me onto your team.

To all the teams I have been part of – thanks. Erkka Laulainen, Markus Hiienkari, and Jukka Teittinen – you were a pleasure to work with. We accomplished a lot together. Thanks to Professor Nikolic at the University of California Berkeley (BWRC) for letting me visit. Thanks to Dr. Hanh-Phuc Le and Dr. Ruzica Jevtic for the DC-DC tips. Thanks to Dr.

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Now on to the folks that kept my day-to-day tasks moving along. Thanks to Artturi Kaila and Dr. Marko Kosunen for keeping the servers (and me) happy. Artturi – you brought me back to earth and reminded me that not everything is related to circuits. I will also miss watching the American ”classics” with you in the break room. Lea Söderman – thanks for helping me with all the practical tasks and helping me to improve my Finnish. Thanks to Anita Bisi, Marja Leppäharju, and Arja Hjelt.

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This work would not have been possible without my wife Tiia. In Chisu's words ... ”sä oot ihana” and deserve my utmost gratitude. You have brought so much happiness to my life! Thanks to Tara for the occasional entertainment at the lab. And to my girls (Isabel, Amelia, and Elinor) ... you mean the world to me! Thanks to my parents, brother, and Grandma for the love and support in all my endeavors. Thanks to Tiia's family for making my time in Finland so special.

Thanks to the guys outside for revving your engines consistently for 5 years. Thanks to Finland for all the opportunities. Thanks to all my friends who reminded me how much fun life is (especially the Suomi crew, Ryan, and Larry). I know I forgot to thank at least a few people. But you know who you are ... so thanks.

In Espoo, December 21, 2015,

Matthew J. Turnquist

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I J. Mäkipää, M.J. Turnquist, Erkka Laulainen, L. Koskinen. Timing-error detection design considerations in subthreshold: an 8-bit microprocessor in 65 nm CMOS. *Journal of Low Power Electronics*, 2, pp. 180-196, May 2012.

II M.J. Turnquist, G. de Streel, D. Bol, M. Hiienkari, L. Koskinen. Effects of back-gate bias on switched-capacitor DC-DC converters in UTBB FD-SOI. In *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, San Francisco, California, October 2014.

III M.J. Turnquist, M. Hiienkari, J. Mäkipää, H.-P. Le, L. Koskinen. Rethinking DC-DC converter design constraints for adaptable systems that target the minimum-energy point. In *Symposium on Low Power Electronics and Design (ISLPED)*, Beijing, China, pp. 383-388, September 2013.

IV M.J. Turnquist, E. Laulainen, J. Mäkipää, M. Pulkkinen, L. Koskinen. Measurement of a timing error detection latch capable of subthreshold operation. In *NORCHIP Circuit Conference*, Trondheim, Norway, November 2009.

V M. Hiienkari, J. Mäkipää, M.J. Turnquist, J. Teittinen, A. Rantala, M. Sopanen, M. Kaltiokallio, L. Koskinen. A 3.15pJ/cyc 32-bit RISC CPU

with timing-error prevention and adaptive clocking in 28 nm CMOS. In *Custom Integrated Circuits Conference (CICC)*, San Jose, CA, pp. 1-4, September 2014.

VI M.J. Turnquist, E. Laulainen, J. Mäkipää, L. Koskinen. Measurement of a System-Adaptive Error-Detection Sequential Circuit with Subthreshold SCL. In *NORCHIP Circuit Conferenc*, Lund, Sweden, pp. 1-4, November 2011.

VII M.J. Turnquist, M. Hiienkari, J. Mäkipää, L. Koskinen. A Fully Integrated Self-Oscillating Switched-Capacitor DC-DC Converter for Near-Threshold Loads. In *Asian Solid-State Circuits Conference (A-SSCC)*, Xiamen, China, pp. TBD, November 2015.

VIII M.J. Turnquist, M. Hiienkari, J. Mäkipää, R. Jevtic, E. Pohjalainen, T. Kallio, L. Koskinen. Fully Integrated DC-DC Converter and a 0.4V 32-bit CPU with Timing-Error Prevention Supplied from a Prototype 1.55V Li-ion Battery. In *Symposium on VLSI Circuits*, Kyoto, pp. c320-c321, June 2015.

IX L. Koskinen, M. Hiienkari, J. Mäkipää, M.J. Turnquist. Implementing Minimum-Energy-Point Systems with Adaptive Logic. In *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, July 2015.

X K. Östman, M.J. Turnquist, K. Stadius, L. Koskinen, J. Ryynänen. Supply Ripple Analysis for Receiver Front-Ends Powered by Fully Integrated DC-DC Converters. *IEEE Transactions on Power Electronics*, (submitted) April 2015.

Author's Contribution

Publication I: "Timing-error detection design considerations in subthreshold: an 8-bit microprocessor in 65 nm CMOS"

The author designed the reported EDS circuit and wrote the paper manuscript. Mr. Mäkipää and Mr. Laulainen designed the microprocessor. The author assisted Mr. Laulainen in the EDS circuit measurements. Dr. Koskinen supervised the work.

Publication II: "Effects of back-gate bias on switched-capacitor DC-DC converters in UTBB FD-SOI"

The author designed the SC DC-DC converter, assisted in the switch and control circuitry analysis, and wrote the manuscript. Mr. de Streel assisted in the switch and control circuitry analysis. Dr. Bol and Dr. Koskinen supervised the work.

Publication III: "Rethinking DC-DC converter design constraints for adaptable systems that target the minimum-energy point"

The author performed the majority of the circuit analysis, wrote the paper manuscript, and presented the paper. Dr. Le assisted with the circuit analysis and revision of the manuscript. Mr. Mäkipää and Mr. Hiienkari reviewed the manuscript. Dr. Koskinen supervised the work.

Publication IV: "Measurement of a timing error detection latch capable of sub-threshold operation"

The author designed the reported EDS circuit, wrote the paper manuscript, and presented the paper. Mr. Mäkipää and Mr. Laulainen designed the combinational logic. Mr. Laulainen and Mr. Pulkkinen assisted in the system measurements. Dr. Koskinen supervised the work.

Publication V: "A 3.15pJ/cyc 32-bit RISC CPU with timing-error prevention and adaptive clocking in 28 nm CMOS"

Markus Hiienkari designed and implemented the majority of the digital parts of the system, and wrote test software and the manuscript. The author assisted in the optimization of the TBD cell.

Publication VI: "Measurement of a System-Adaptive Error-Detection Sequential Circuit with Subthreshold SCL"

The author designed the reported EDS circuit, wrote the paper manuscript, and presented the paper. Mr. Mäkipää and Mr. Laulainen assisted in the uncertainty region model. Dr. Yücetaş assisted in the layout. The author assisted Mr. Laulainen in the EDS circuit measurements. Dr. Koskinen supervised the work.

Publication VII: "A Fully Integrated Self-Oscillating Switched-Capacitor DC-DC Converter for Near-Threshold Loads"

The author designed the reported DC-DC converter, performed the circuit analysis, and wrote the paper manuscript. Mr. Hiienkari assisted in the measurements. Mr. Mäkipää and Mr. Hiienkari reviewed the manuscript. Dr. Koskinen supervised the work.

Publication VIII: "Fully Integrated DC-DC Converter and a 0.4V 32-bit CPU with Timing-Error Prevention Supplied from a Prototype 1.55V Li-ion Battery"

The author designed the reported DC-DC converter and assisted in system measurements with Mr. Hiienkari. The author wrote the paper

manuscript. The author measured the DC-DC and Mr. Hiienkari and Mr. Mäkipää measured the CPU. The battery was designed and measured by Mrs. Pohjalainen and Dr. Kallio. Dr. Jevtic and Dr. Koskinen supervised the work.

Publication IX: "Implementing Minimum-Energy-Point Systems with Adaptive Logic"

The author designed the reported DC-DC converter and assisted in the system simulations. The manuscript was written by Dr. Koskinen. The TEP adaptive load was designed by Mr. Hiienkari. Mr. Mäkipää and Dr. Koskinen supervised the work.

Publication X: "Supply Ripple Analysis for Receiver Front-Ends Powered by Fully Integrated DC-DC Converters"

The author designed the reported DC-DC converter. The author performed the ripple analysis and measurement results in Section II. The author wrote Section II and Dr. Östman wrote the remainder of the paper manuscript. Dr. Mikko Kaltiokallio assisted in the layout of the DC-DC converter. Dr. Stadius, Dr. Koskinen, and Prof. Ryynänen supervised the work.

List of Symbols

A	area
C_{fly}	flying capacitance
E_L	leakage energy
E_{SW}	switching energy
E_{SYS}	system energy per operation
E_T	total energy
f_{SW}	DC-DC converter switching frequency
f_T	transition frequency at the asymptotic intersection of the SSL and FSL impedances
G_{ON}	switch on-conductance
G_{tot}	summed switch on-conductance
I_{OUT}	output current
K_{OCR}	optimal conversion ratio factor
L	length of a transistor
MEP_{SYS}	system minimum energy per operation point
N_{MP}	number of multiphase interleaved units
N	voltage conversion ratio
P_{Cfly}	inherent SC losses
P_{IN}	input power
$P_{OUT,max}$	maximum output power
$P_{OUT,min}$	minimum output power
$P_{OUT,ratio}$	ratio of maximum output power to minimum output power
P_{OUT}	output power
$P_{bott-cap}$	bottom-plate losses
P_{cond}	switch conductance losses
P_{cont}	control circuitry losses

$P_{gate-cap}$	gate-plate losses
P_{loss}	DC-DC converter losses
R_{FSL}	fast switching limit output impedance
R_L	load impedance
R_{SSL}	slow switching limit output impedance
R_o	DC-DC converter impedance
$VBBN$	back-gate voltage applied to NMOS
$VBBP$	back-gate voltage applied to PMOS
V_{BAT}	battery input voltage
V_{DD}	output voltage with a processor load
V_{DIFF}	output voltage of the SC subtractor
V_{IN}	input voltage
$V_{OUT,OPT}$	output voltage at the MEP
V_{OUT}	output voltage
V_{gs}	gate-source voltage of a transistor
V_{th}	threshold voltage of a transistor
W	width of a transistor
ΔV_{OUT}	peak-to-peak ripple at V_{OUT}
α_v	velocity saturation index
α	processor activity factor
η_{lin}	efficiency of an ideal linear regulator
η_{max}	maximum conversion efficiency
η_{min}	minimum conversion efficiency over specified load range
η	conversion efficiency
ϕ_{charge}	charge phase
$\phi_{discharge}$	discharge phase

List of Abbreviations

CMOS	complimentary metal-oxide-semiconductor
EEF	efficiency enhancement factor
FBB	forward body bias
FSL	fast switching limit
IC	integrated circuit
ITRS	international technology roadmap for semiconductors
iVCR	ideal voltage conversion ratio
LDO	low drop out regulator
LVT	low threshold voltage
MEP	minimum energy point
MOM	metal-oxide-metal
NMOS	n-type metal oxide semiconductor
NOC	non-overlapping clock generator
NT	near-threshold
oVCR	optimal voltage conversion ratio
PD	power density
PFM	pulse frequency modulation
PMOS	p-type metal oxide semiconductor
PMU	power management unit
PVTA	process, voltage, temperature, and ageing
RBB	reverse body bias
RVT	regular threshold voltage
SC	switched-capacitor
SCL	source-coupled logic
SCN	switched-capacitor network
SIR	scaled-input regulation
SSL	slow switching limit

STSCL	sub-threshold source-coupled logic
TED	timing-error detection
TEP	timing-error prevention
ULE	ultra-low-energy
ULV	ultra-low-voltage
UTBB FD-SOI	ultra-thin buried oxide and body fully-depleted silicon-on-insulator
VCR	non-ideal voltage conversion ratio

1. Introduction

As the size of electronics continues to decrease and the functionality requirements increase, energy consumption is becoming a critical issue. This is especially true for ultra-portable electronics such as smart watches, fitness tracking bracelets, smart rings, contact lenses, and smartdust (Fig. 1.1 (a)). Unfortunately, battery energy density has developed slowly relative to the energy needs of these devices. To make matters worse, battery energy density does not scale well with smaller sizes [1]. Consequently, there is a growing energy gap between energy needed and energy available. Harvesting techniques do help and can even allow for energy-autonomous operation in some ultra-portable applications [2–5]. However, circuit-level solutions are still critical in these applications and in the development of future ultra-portable electronics [6].

As shown in Fig. 1.1 (b), an integrated circuit (IC) for ultra-portable electronics has four main blocks: (i) sensing, (ii) data processing, (iii) communication, and (iv) a power management unit (PMU). The PMU is the interface between the energy source and all of the blocks. The tasks of the PMU include DC-DC conversion, energy source harvesting/monitoring, and power gating [7]. Of the four blocks, communication (through data transmission) has the potential to consume a large proportion of the overall energy. Unfortunately, within a wireless node, the energy consumption needed to transmit a bit does not scale with Moore's law as advantageously as with digital processing. Thus, there is strong motivation to minimize the amount of transmitted data by increasing the amount of ultra-low-energy (ULE) intra-node processing.

Scaling the supply voltage with complimentary metal-oxide-semiconductor (CMOS) technology has been historically used to decrease energy per operation of data processing blocks. However, according to the international technology roadmap for semiconductors (ITRS) the impact of supply volt-

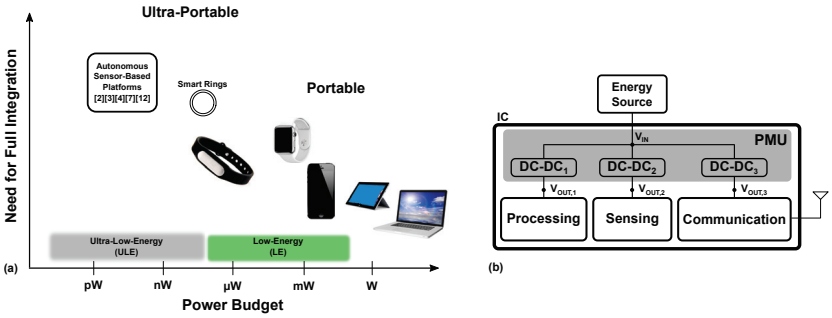


Figure 1.1. (a) Relationship between power budget and the need for full integration; (b) Typical IC architecture for an ultra-portable application.

age scaling is minimal for sub–90 nm technology [8]. This stagnation in nominal voltage scaling has motivated a strong interest in operating at near-threshold (NT) voltages. Operating at NT significantly reduces energy consumption but avoids the large variance and performance penalties of sub-threshold [9, 10]. The increasing focus on ULE processing also means an increased importance in the DC-DC converter (*i.e.* DC-DC$_1$ in Fig. 1.1 (b)).

In a typical ultra-portable device, the processing block's (NT) supply voltage is supplied by a DC-DC converter with a system supply or battery input as shown in Fig. 1.1 (b). There are two main constraints for the DC-DC converter in this ULE system. First, high efficiency is of utmost importance. Based on state-of-the-art DC-DC converters [11], an efficiency over 75 % is considered high efficiency in this thesis. The energy consumption of the DC-DC converter/processor system is proportional to the efficiency of the DC-DC converter. In other words, saving energy in the processing block by scaling to NT voltages is only worthwhile if the DC-DC converter supplying the NT voltage is efficient. The second constraint for the DC-DC converter is that it needs to be fully integrated due to the increasingly small form factors of typical ultra-portable devices [2, 12].

In order to meet the efficiency and size constraints, the DC-DC converter needs to be designed by keeping in mind the fact that processors operating at NT voltages have significantly different characteristics than during traditional super-threshold operation. Processors operating at such ultra-low-voltage (ULV) typically have adaptivity to combat the high delay sensitivity to variations. The adaptivity can be used to the advantage of the DC-DC converter. A DC-DC converter supplying an ULV processor must be capable of maintaining high efficiency over a large load power range [13] since toggling between active and sleep modes can produce from 200x

[14] to 6000x [15] changes in load power. Sleep mode power levels are particularly challenging due to control circuitry losses [16].

In general, a DC-DC converter designed for a super-threshold load does not necessarily function efficiently for a sub- or near-threshold voltage load. Here in this work, we explore how to make the DC-DC converter work well specifically with an ULE load operating at NT voltages. Ensuring that these two blocks operate efficiently together minimizes energy consumption, and ultimately, helps in enabling ultra-portable electronics.

For the processing block, the DC-DC converter is typically a linear-mode or switched-mode converter. There also exists hybrid linear/switched - mode converters [17–19]. Linear-mode converters are typically an low drop out regulator (LDO). The LDO is not an ideal choice since its efficiency is limited to the ratio of V_{OUT} over V_{IN}. Even with a low V_{IN} of 1 V, down-converting to an (NT) voltage of 0.3 V with an LDO would give an efficiency of only 30 %.

Switched-mode converters are a well-suited choice for meeting the demands of ULE processors [5, 14, 20, 21]. They can provide high efficiency over a large range of output voltages and power levels. Switched-mode converters transfer energy from the input to the output using passive components and switches. When the passive component is a capacitor (inductor), the converter is called a switched-capacitor (switched-inductor) converter. In terms of power density, efficiency, and scaling, switched-capacitor (SC) DC-DC converters are a more promising choice than switched-inductor converters for achieving full integration. The main reasons behind this choice are the fact that capacitors have 10-100 times more energy per volume than inductors and that SC converters have improved switch utilization [22–25].

In this work, we explore the characteristics of fully integrated SC DC-DC converters designed for ULE adaptive processors. Overall, decreasing the system energy consumption is the focus throughout the work. We present a number of approaches to reduce the system energy consumption: new DC-DC topologies, new regulation techniques, operation with a prototype Li-ion battery, and utilization of back-gate biasing (within UTBB FD-SOI).

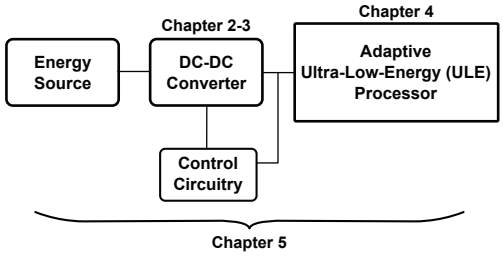


Figure 1.2. Organization of the thesis.

1.1 Objective of the Thesis

The objective of this thesis is to answer the following questions:

1. What are the DC-DC converter design constraints for ULE processors?

2. What are the co-design considerations of a DC-DC converter/processor system?

These questions will be answered within the thesis by analysis in three main areas: (i) SC DC-DC converters, (ii) ULE processors, and (iii) DC-DC converter/processor systems.

1.2 Organization of the Thesis

This thesis consists of two parts. Firstly, an introduction with five chapters is given. Secondly, a compilation of scientific publications ([I]-[X]) by the author is given. The six chapters within the introduction describe the necessary SC converter background, implemented designs, and comparison to state-of-the-art DC-DC converters. More specifically, chapter 2 provides the SC DC-DC converter background relevant to ULE processors. Chapter 3 describes the implementation of three fully integrated SC DC-DC converters with ULE loads. Chapter 4 examines the behavior of ULE processors. The system effects of the DC-DC converter and ULE processor loads are then given in chapter 5. Finally, a conclusion in chapter 6 summarizes the findings of the thesis and compares the implemented DC-DC converters to the state-of-the-art.

1.3 Main Scientific Contributions

The scientific contributions of this work are presented in detail within publications [I]-[X]. A summary of the work in these publications is found in chapters 2-6 of this thesis. The most important scientific contributions from the publications can be further summarized as:

1. A design approach to improve DC-DC converter efficiency over a large load range by using a new topology and back-gate biasing. At the time of publication, this DC-DC converter had the highest power density for a fully integrated NT converter and is the first-known implementation of the self-oscillating step-down topology [VII].

2. Designed the first-known EDS circuit capable of sub-threshold operation [IV].

3. A fully integrated Dickson DC-DC converter. It is the first-known fully integrated version of this topology [VIII].

4. Implemented an EDS circuit in sub-threshold source-coupled logic [VI]. This EDS circuit is used within the first-known timing-error detection (TED) processor capable of sub-threshold operation [I].

5. A design approach for improving DC-DC converter efficiency by using back-gate biasing in order to reduce control circuitry leakage energy [VIII].

6. A technique utilizing back-gate biasing in order to reduce switch sizes and improve DC-DC converter efficiency [II].

7. A design approach for reducing energy consumption of a battery/DC-DC converter/CPU system. The battery is a 1.55 V Li-ion prototype. At the time of publication, this system had the lowest reported energy per operation [VIII].

8. Identified key ripple characteristics of SC converters [X].

9. A DC-DC converter regulation methodology to reduce (battery/DC-DC converter/CPU) system energy consumption [III, IX].

10. A method to detect the threshold voltage with a DC-DC converter and a TED processor (chapter 6).

2. Switched-Capacitor DC-DC Converters

This chapter provides the relevant background information on SC DC-DC converters. The focus is on SC DC-DC converters that supply energy-constrained NT processor loads. The main principles, operation characteristics, and a description of the switched-capacitor network (SCN) are given. Finally, the most relevant implementation parameters are considered.

2.1 Principles

A common method to model an SC DC-DC converter is with the SC output impedance model [22, 26, 27]. This model (Fig. 2.1) consists of a transformer and a series resistance (R_o). The transformer represents the converter's ideal voltage conversion ratio (iVCR). The iVCR is expressed as:

$$iVCR = V_{NL}/V_{IN} = 1/N, \tag{2.1}$$

where V_{NL} is the no-load voltage after conversion and N is the conversion ratio of the transformer. For example, the divide-by-two and divide-by-three converters presented in the next chapter have $iVCRs$ of 1/2 and 1/3,

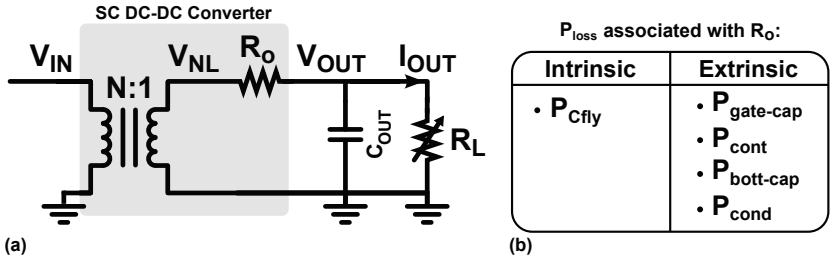


Figure 2.1. (a) SC output impedance model [22, 26, 27] and (b) the losses associated with R_o.

respectively. The iVCR is determined solely by the converter SCN topology. When a load is connected to the converter, the output voltage V_{OUT} decreases below V_{NL} and the non-ideal voltage conversion ratio (VCR) is given by:

$$VCR = \frac{V_{OUT}}{V_{IN}} \tag{2.2}$$

The decrease in the output voltage V_{OUT} below V_{NL} is modeled by the output impedance R_o. This impedance has a dual nature; it depends on the contributions from the slow switching limit (SSL) and fast switching limit (FSL). The SSL impedance is due to capacitor-dominated losses and the FSL impedance results from resistive losses [23, 28]. The SSL and FSL have asymptotic behavior, and there is a transition frequency (f_T) at the intersection of the two asymptotes [26]. R_o is given by the following equations in terms of SSL and FSL [25]:

$$R_o = \sqrt{(R_{SSL})^2 + (R_{FSL})^2} = \sqrt{\underbrace{(\frac{K_c}{C_{tot} f_{SW}})^2}_{R_{SSL}} + \underbrace{(\frac{2K_s}{G_{tot}})^2}_{R_{FSL}}}, \tag{2.3}$$

where K_c and K_s depend on the topology, C_{tot} is the total fly capacitance, f_{SW} is the converter switching frequency, and G_{tot} is the summed switch on-conductance.

Understanding the losses associated with R_o is crucial for achieving high conversion efficiency within the DC-DC converter. The losses are both intrinsic and extrinsic. The intrinsic losses (P_{Cfly}) arise from charging a capacitor through a switch [22]. Extrinsic losses within the converter are due to implementation, and they can be grouped into four loss mechanisms. First, the bottom-plate losses ($P_{bott-cap}$) arise from the parasitic capacitance to the substrate of the fly capacitors and switches. Second, the gate capacitance switching losses ($P_{gate-cap}$) are caused by charging and discharging the gates of the switches. Third, the control circuitry losses (P_{cont}) come from any control circuitry used to operate and/or regulate the converter. Fourth, the conduction loss (P_{cond}) arises from the finite conduction of the switches. The sum of both intrinsic and extrinsic losses can be summarized as:

$$P_{loss} = P_{Cfly} + P_{bott-cap} + P_{gate-cap} + P_{cont} + P_{cond} \tag{2.4}$$

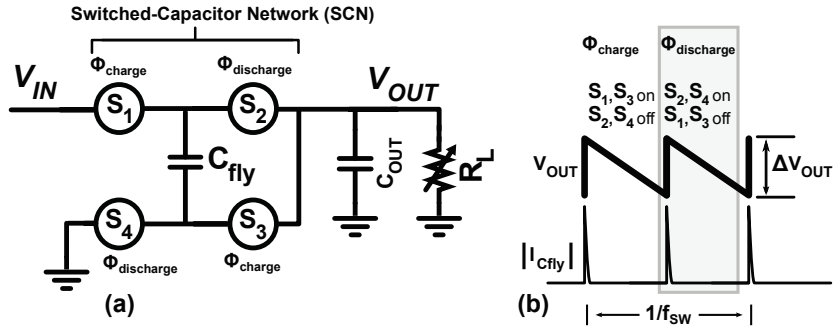


Figure 2.2. 2:1 series-parallel SC converter (a) circuit and (b) operation.

2.2 Operation Characteristics

To illustrate the operation of an SC DC-DC converter, the circuit and transient behavior of a 1/2 series-parallel DC-DC converter are shown in Fig. 2.2 (a) and (b), respectively. SC converters have an SCN composed of switches and capacitors. The switches typically operate with two phases and with a 50 % duty cycle. Although it is possible to operate SC DC-DC converters with different duty cycles, a 50 % duty cycle has been shown to be optimal for two-phase switching [22]. During the charge phase (ϕ_{charge}), charge is stored on the fly capacitor C_{fly} and flows to the load. The stored charge on C_{fly} flows to the load during the discharge phase ($\phi_{discharge}$). The output capacitor (C_{OUT}) does not contribute to charge transfer with respect to the conversion, it only reduces the ripple (ΔV_{OUT}) at V_{OUT}.

The speed of charge transfer, or f_{SW}, has a direct impact on the R_o impedance as seen from (2.3). In SSL, the R_o is inversely proportional to f_{SW}. In FSL, the f_{SW} has a minimal impact on R_o unless f_{SW} is much higher than f_T [26].

2.3 Switched-Capacitor Network

As shown previously, an SC DC-DC converter is composed of an SCN. In the following text, we examine the design choices of the capacitors and switches that form the SCN.

Capacitors

The type of fly capacitor has three important effects on the converter design. First, the fly capacitor's capacitance density largely determines the

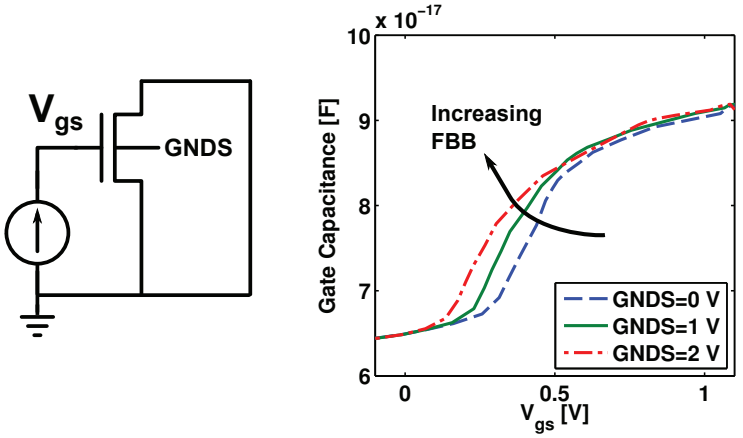


Figure 2.3. Capacitance plot for an NMOS transistor in 28 nm UTBB FD-SOI.

total converter area since the area of the fly capacitor dominates the design. The converter designs in [X], [VIII], and [VII], and other state-of-the-art implementations, confirm the previous statement. Second, the losses due to bottom plate parasitic ($P_{bott-cap}$) limits the efficiency of the converter at power levels used within this thesis. The third effect stemming from the choice of fly capacitor is functionality since some capacitors (*e.g.* MOSCAPs), have voltage dependencies.

Depending on the process technology, multiple types of capacitors may be available. A qualitative summary of different fly capacitor choices for an integrated DC-DC converter is shown in Table 2.1. Deep trench capacitors, which are built with embedded DRAM process options [29], are an excellent choice to their high capacitance density [30, 31]. However, deep trench capacitors are still an exotic technology and not standard components in current CMOS technologies. MIMs, which are standard components in most current digital CMOS technology, are the next best choice for NT converters since they have low $P_{bott-cap}$, do not have voltage dependencies, and have a medium capacitance density. Since MIMs are formed between two high metal layers and a thin dielectric, the area can also be utilized underneath them to increase their effective density [14].

For NT converters, the use of MOSCAPs for the fly capacitor is typically avoided [32]. A MOSCAP, which is formed between the gate and the induced channel of a MOS transistor [33], has a capacitance density that decreases for capacitor voltages below V_{th} as shown in Fig. 2.3. Applying forward body bias (FBB) to reduce V_{th} does help slightly in shifting the capacitance decrease to lower V_{gs}. This improvement is, however, still not

	MIM	MOSCAP	CMOM	Deep Trench
Voltage Dependency?	No	Yes	No	No
Capacitance Density	Medium	High	Low	High
Bottom Plate Parasitics ($P_{bott-cap}$)	Low	*High	Medium	Low
Circuits Underneath?	Yes	No	Yes	Yes

*This is decreased with SOI transistors

Table 2.1. Fly capacitor choices for fully integrated SC converters.

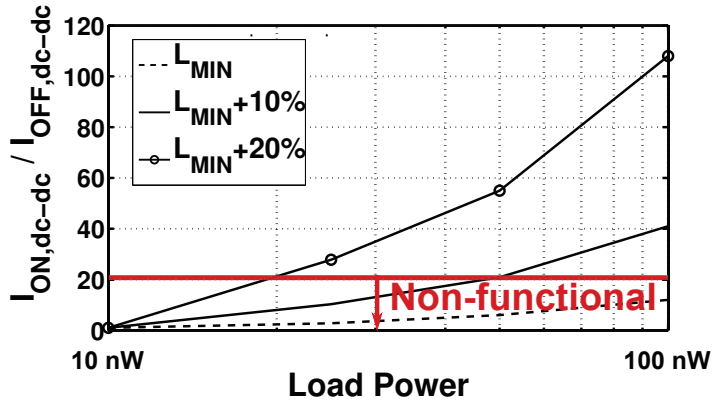


Figure 2.4. Simulation results from [II] showing the impact of leakage on a 2:1 DC-DC converter with sleep mode load power. ©2014 IEEE

adequate since the V_{gs} of a MOSCAP would still see only a fraction of the NT output voltage (*e.g.* 0.1 V to 0.2 V). Additional challenges with leakage also limit this approach. Avoiding the use of MOSCAPs is one reason why it is challenging for NT converters to have comparable power densities to the super-threshold converters. In summary, the capacitor choice has a large impact on the overall design of NT converters. As further described in chapter 3, the implemented converters in this thesis use metal-oxide-metal (MOM) [X] and MIM [VIII], [VII] fly capacitors.

Switches

Switches are used to transfer charge to and from the fly capacitors (C_{fly}). Switches require more attention in low power designs for two reasons. First, drain-source leakage in the switches can cause functionality problems at small load power [II] or when the converter needs to be powered *OFF* [34]. As shown in Fig. 2.4, the switches within a 2:1 DC-DC converter require a minimum ratio of *ON*-current ($I_{ON,dc-dc}$) to *OFF*-current

($I_{OFF,dc-dc}$) in order to maintain functionality at nW power levels. Increasing the L reduces leakage with a tradeoff in increased losses at active mode load power levels.

The second reason switches require more attention is that achieving adequate switch transconductance is challenging due to a low overdrive voltage [26]. Low overdrive voltage is a result of low V_{gs} as discussed in [VII]. Increasing transistor width (W) may help with increasing the overdrive voltage but it also increases the drain-source leakage and increases the switch driving losses. This tradeoff is especially important to consider for large load power ranges.

2.4 Implementation Parameters

Efficiency

For energy-constrained processors, (power conversion) efficiency is one of the foremost important metrics. The energy consumption of a DC-DC converter/processor system is proportional to the efficiency of the converter. Efficiency is the ratio of the converter's output power (P_{OUT}) and the input power (P_{IN}) as follows:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{loss} + P_{OUT}} \tag{2.5}$$

where P_{loss} is the converter's losses previously defined in (2.4). The maximum efficiency is bound the ratio of the VCR and the iVCR [26] as follows:

$$\eta_{max} = \frac{VCR}{iVCR} = \frac{V_{OUT}}{V_{NL}} = \frac{NV_{OUT}}{V_{IN}} \tag{2.6}$$

The VCR at which η_{max} occurs is defined as the optimal voltage conversion ratio optimal voltage conversion ratio (oVCR):

$$oVCR = K_{OCR} * V_{NL} \tag{2.7}$$

where K_{OCR} is the optimal conversion ratio factor and is always less than one. Typically, K_{OCR} varies from 80 % to 95 % depending on a number of factors (*e.g.* load, topology, etc.).

The minimum conversion efficiency over a specified load range is defined as η_{min}. A high η_{min} over a large load range is highly desirable for ULE adaptive processors that have sleep and active modes (that induce large changes in load power).

Efficiency Enhancement Factor

As presented in (2.6), the maximum efficiency (η_{max}) in an SC converter is bound by VCR/iVCR. The η_{max} only accounts for the converted output voltage. Additional intrinsic and extrinsic losses as shown in (2.4) reduce the actual efficiency. These losses typically increase as the VCR decreases (to achieve a higher down-conversion), and thus, efficiency in SC converters is proportional to VCR [35]. To account for this effect, and to benchmark against a linear-mode converter, the efficiency enhancement factor (EEF) [33] can be used as a figure of merit:

$$EEF = 1 - \frac{\eta_{lin}}{\eta}, \tag{2.8}$$

where η_{lin} is the efficiency of an ideal linear-mode converter. The linear-mode converter has the same V_{OUT} and V_{IN} as the SC converter. A positive EEF indicates that the efficiency (η) of the SC converter, is improved over an equivalent linear-mode converter.

Load Power Range

The converter needs to function efficiently from the load's minimum power ($P_{OUT,min}$) to maximum power ($P_{OUT,max}$). This load power range can also be expressed as a ratio:

$$P_{OUT,ratio} = P_{OUT,max}/P_{OUT,min} \tag{2.9}$$

The $P_{OUT,ratio}$ for a DC-DC converter is typically orders-of-magnitude for energy-constrained processors [5, 14, 15] that utilize multiple power modes (*e.g.* sleep and active modes) [13].

Ripple

SC DC-DC converters exhibit inherent ripple in their output voltage (V_{OUT}) due to pulse-like current patterns as shown previously in Fig. 2.2. The ripple magnitude of an SC DC-DC converter's output voltage can be understood by assuming that the converter operates in SSL. The worst-case ripple amplitude is expected in SSL, because the parasitic resistances of the switches, capacitors, and interconnects are neglected, and the charge transfer is thus not damped by these parasitics. A general SSL approximation for ripple can be described by rearranging the classic switched-

	Li-ion Prototype [36]	NiMH	Li-ion	Li-ion Polymer	Alkaline
Nominal Voltage	1.55V	1.2V	3.6V	3.6V	1.5V
Voltage over 95% of Discharge Time	1.5V-1.6V	~1.1V-1.3V	~3V-4V	~3V-4V	0.9V-1.5V
Gravimetric Energy Density (Wh/kg)	20	60-120	110-160	100-130	80
Volumetric Energy Density (Wh/l)	925	140-300	270	300	80
Cycle Life (to 80% of initial capacity)	300-400	300-500	500-1000	300-500	50

Table 2.2. Characteristics of modern batteries.

capacitor loss equation in [22] and accounting for multiphase interleaving:

$$\Delta V_{OUT} = \frac{2I_{OUT}}{N_{MP}M_{CAP}f_{SW}C_{fly}} \tag{2.10}$$

where I_{OUT} is the output current into R_L, N_{MP} is the number of multiphase interleaved units, and M_{CAP} is based on the converter architecture [22]. All three of the DC-DC converters presented in the next chapter had ΔV_{OUT} less than 15% of V_{OUT}.

Battery Input

The majority of current portable electronic systems are powered by batteries. Table 2.2 gives an overview of commonly used rechargeable batteries. The high-energy density found in Li-ion based batteries ensures minimal weight and size. These qualities make them an attractive option for applications like smartphones or smartwatches. Li-ion batteries with a 3.6 V nominal voltage are the most common choice for powering modern portable electronics. However, as discussed in the next paragraph and later in chapter 5, the lower (1.55 V) nominal voltage Li-ion of [36] is advantageous.

Modern portable electronics require that the battery voltage (or system voltage) be efficiently down-converted to the processor's operation voltage (V_{OUT}). When V_{OUT} is at or below NT voltages, the ability to maintain high-efficiency in the converter becomes more challenging due to a larger step-down conversion ratio, or equivalently, a decreased VCR. A smaller VCR requires more switches, capacitors, and control circuitry. As shown in Fig. 2.5, state-of-the-art DC-DC converters typically have lower efficiency at lower VCR.

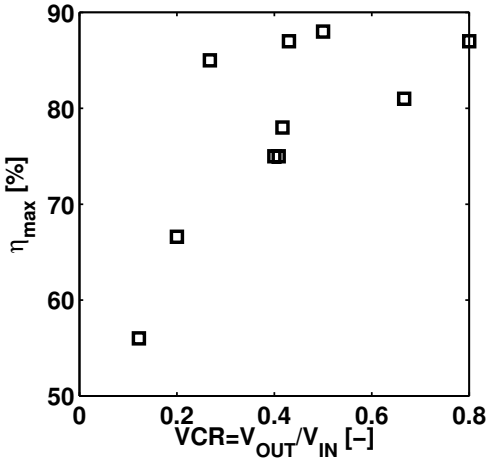


Figure 2.5. Efficiency of state-of-the-art DC-DC converters with various VCRs.

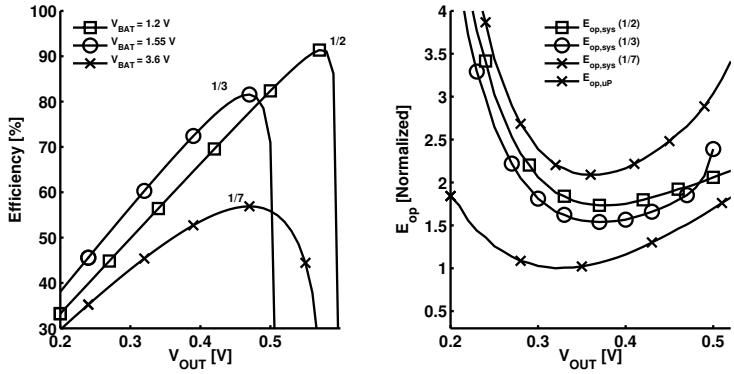
To further clarify the trend in efficiency and VCR, the efficiency of a ladder DC-DC converter in 28 nm CMOS with three topologies is shown in Fig. 2.6 (a). Each topology's iVCR (*i.e.* 1/2, 1/3, and 1/7), is chosen based on the input voltage. As the input voltage is reduced, the required iVCR increases. A larger iVCR requires more switches and capacitors, and thus, there are more extrinsic losses ($P_{bott-cap}$, P_{cont}, and $P_{gate-cap}$). Note that the efficiency curves were generated from the MATLAB model developed in [37]. This model does not take into account P_{cont}. Thus, the efficiency with 1/7 topology would be reduced even further relative to the 1/2 and 1/3 topologies. The subsequent effects of input voltage ultimately effect the energy consumption of a DC-DC converter/processor system as shown in Fig. 2.6 (b). The 1/2 topology has a minimum energy point that gives a 36 % reduction in energy/operation over the 1/7 topology. In summary, choosing the lowest possible input voltage helps to make the DC-DC converter more efficient, and consequently, the DC-DC converter/processor systems operates with lower energy consumption.

Power Density

The cost of a fully integrated DC-DC converter is dependent on its power density (PD). The PD is the output power (P_{OUT}) divided by the silicon area (A) required to perform the conversion

$$PD = \frac{P_{OUT}}{A} \tag{2.11}$$

Achieving high PD is especially challenging for converters that supply NT



(a) (b)

Figure 2.6. (a) A ladder converter with three different topologies (*i.e.* 1/2, 1/3, and 1/7). Each topology is regulating to the NT voltage range from a different input voltage. (b) Effects of the ladder converters' efficiency on a ring oscillator load.

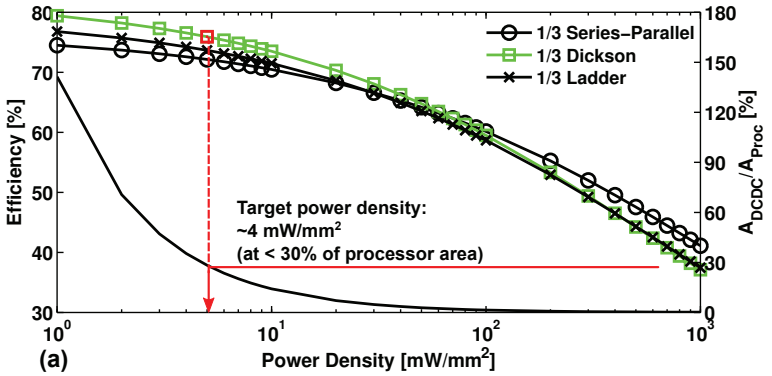
loads for two reasons. The first reason is that NT converters require that the (area-dominant) fly capacitors be constructed from capacitors that are not sensitive to the voltage across them. The only choice is thus MOM or MIM capacitors which have low to medium capacitance density (Table 2.1). Using a MOSCAP, which has a high capacitance density, is not possible due to the drop off in capacitance at NT voltages (see Fig. 2.3). The second reason why it is challenging to achieve PD is that the switches within the SCN have low overdrive voltages at ULV. Using a larger W for switches is one option to compensate for the low overdrive. Nevertheless a larger W means a tradeoff for reduced $P_{OUT,ratio}$ (due to leakage) and decreased efficiency (*e.g.* due to larger $P_{gate-cap}$).

3. DC-DC Converter Prototypes

Previously in the thesis, chapter 2 presented the principles, operation characteristics, and implementation parameters of SC converters. In this chapter, we turn our attention towards three implemented fully integrated SC DC-DC converters. Each converter is designed to convert a system supply or battery voltage down to an NT load. This chapter is divided into three sections. The first section discusses a 3:1 Dickson converter in (bulk) CMOS and the motivation for the Dickson topology. Next, two SC converters built in ultra-thin buried oxide and body fully-depleted silicon-on-insulator (UTBB FD-SOI) CMOS are presented. The necessary background and motivation for using UTBB FD-SOI CMOS is also discussed.

In this chapter, the author's contributions focus specifically on using high-efficiency DC-DC converters for energy-constrained processors that operate at NT voltages. These DC-DC converters serve a critical role since energy consumption of a DC-DC converter/processor system is proportional to the DC-DC converter's conversion efficiency. In other words, scaling a processor's supply voltage to NT is only worthwhile if the DC-DC converter can operate with high efficiency. This high conversion efficiency must also be maintained over a wide load power range since toggling between a processor's sleep and active mode can produce up to 6000 x [15] changes in load power. While the first converter (in section 3.1) is focused on efficiency, the final two converters (in section 3.2) explore new methods of providing a high efficiency over a wide load power range. A performance summary is given for each of these three converters.

This chapter highlights the most significant aspects of the original work. Further analytic and implementation details can be found in the related scientific publications: [VII], [VIII], and [X].



(b)

	1/3 Ladder	1/3 Dickson	1/3 Series-Parallel
M_{SW}	18	24.5	24.5
M_{bott}	0.98	1	2.5
M_{cap}	$0.\overline{8}$	$1.\overline{3}$	1.6
Num. of fly caps	3	2	2

Figure 3.1. (a) Efficiency of three divide-by-three topologies based on equations from [22]. The target PD is based on an area constraint with respect to the processor area. (b) Constants need to calculate efficiency in [22].

3.1 3:1 Dickson DC-DC Converter in Bulk 28 nm

Introduction

The main requirement of the 3:1 Dickson converter is to efficiently convert from a battery input voltage range (V_{IN}) down to NT voltages (for a processor load). The area of the DC-DC converter (A_{DCDC}) is required to be 30% less than the area of the processor load (A_{Proc}). The processor load is the same as in [V]. V_{IN} was chosen based on the voltage range of a prototype 1.55 V battery [38].

To choose the best DC-DC converter topology based on the requirements discussed previously, the efficiency of a ladder, a Dickson, and a series-parallel topology are calculated using equations from [22]. A plot of these efficiency results as a function of power density is shown in Fig. 3.1 (a). Constants (M_{SW}, M_{bott}, and M_{cap}) are needed in calculating the efficiency of each topology (3.1 (b)); details of these constants are given in [22]. The Dickson step-down topology, which was first introduced in [39] with off-chip fly capacitors, has the highest efficiency for the target PD.

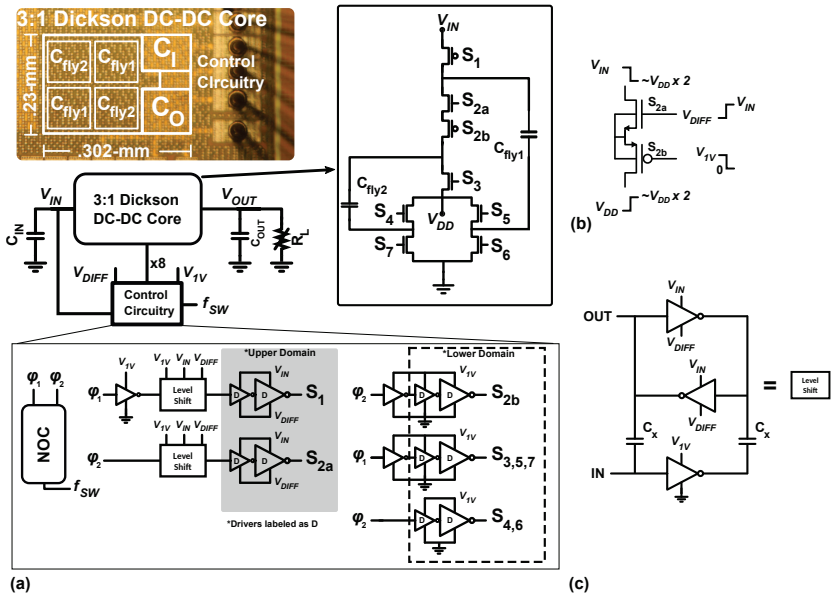


Figure 3.2. (a) Implementation of the 3:1 Dickson converter from [X]. ©2015 IEEE. (b) Details of $S_{2,a,b}$. (c) Capacitive level shifter.

Circuitry

The 3:1 Dickson converter is implemented in 28 nm bulk CMOS. The converter consists of a core and control circuitry as shown in Fig. 3.2. The core has eight switches (S_{1-8}) and two fly capacitors ($C_{fly1,2}$). A two-phase non-overlapping clock generator (NOC) generates the switches' control signals. These signals are input to drivers (D) that form tapered buffers [40, pp. 344-345]. V_{DIFF} is an auxiliary source equal to V_{IN}-1 V. S_{2a} and S_{3-7} are triple-well n-type metal oxide semiconductor (NMOS) transistors and S_1 and S_{2b} are p-type metal oxide semiconductor (PMOS) transistors. The switches and fly capacitors within the core are optimized for high efficiency according to [22].

The NMOS/PMOS stack for $S_{2a,b}$, as shown in Fig. 3.2 (b), was the most challenging switch to design due to the V_{IN}-V_{OUT} voltage drop across the switch during the time it was *OFF*. The NMOS/PMOS stack ensures control voltages less than the breakdown voltage and reduced leakage when $S_{2a,b}$ is *OFF*.

To ensure that S_1, S_{2a} and the drivers of S_1 and S_{2a} can be built with thin-oxide transistors, rather than (inefficient) thick-oxide I/O devices, the gates of S_1 and S_{2a} need to switch at the upper domain (*i.e.* between V_{BAT} and V_{DIFF}). Switching in the upper domain does not violate the breakdown voltage of a thin-oxide transistor. Level shifters are used to

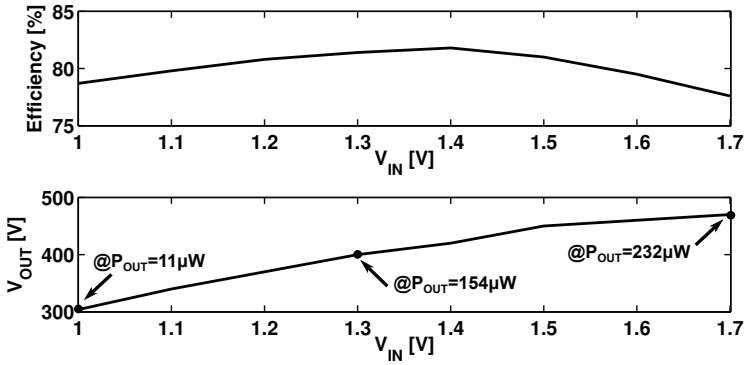


Figure 3.3. Simulation results of the 3:1 Dickson converter. For this simulation, the VCR is fixed at 0.3.

translate the control signals of the lower domain (*i.e.* between V_{1V} and 0 V) to the upper domain. The (capacitive) level shifter [22, 41], which also uses thin-oxide transistors, is shown in Fig. 3.2 (c).

The fly capacitors are custom MOMs with a vertical parallel plate structure [42] utilizing metal layers M2 to M8. This choice of metal layers provided a good tradeoff between capacitor density and $P_{bott-cap}$. The capacitor density was estimated (from HFSS and parasitic extraction) to be 5 fF/μm^2 and $P_{bott-cap}$ to be 1.2 %. MIMs would have been preferred due to their superior performance (Table 2.1), however, at the time of implementation, they were not available.

Measurement Results

The performance of the converter was characterized through simulations and measurements. As shown in Fig. 3.3, the converter achieves high (simulated) efficiency at NT output voltages. The VOCR (V_{OUT}/V_{IN}) was fixed in the simulation at 0.3 V. In other words, the (open-loop) converter produced V_{OUT}=304 mV to 470 mV from V_{IN}=1 to 1.7 V. The technique of scaling the V_{OUT} with V_{IN} is called scaled-input regulation (SIR) and is further discussed in chapter 5. For the target 1.55 V battery input, the Dickson converter achieves 80 % efficiency as shown in Fig. 3.3.

The load used in the previous results was a current source load as shown in Fig. 3.4. It was used to mimic the processor's average current (I_{avg}), leakage current (I_{leak}), and peak current spikes (I_{spike}). The load profile for was built from both ring oscillator simulations and synthesis results.

The Dickson converter was implemented and measured. In the measurements, the converter operated correctly with the on-chip processor

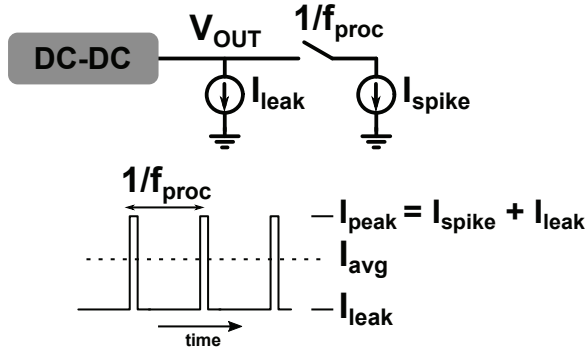


Figure 3.4. Simulation test setup for a processor load.

from [V]. The measurement results with this processor and a 1.55 V battery input are described in [43]. However, a suspected error in the pads and/or wirebonding meant that it was not possible to measure the efficiency.

Although the converter efficiency could not be measured, measurements of the voltage ripple magnitude as a function of the switching frequency (f_{SW}) were possible as shown in Fig. 3.5. This measurement was performed at the $P_{OUT,min}$ (14 μW) and $P_{OUT,max}$ (115 μW). The ripple was less than 12 % of V_{OUT} for both power levels. The analytically predicted ripple, which was calculated with an optimal switching frequency ($f_{SW,OPT,l}$) inserted into (2.10), closely matched the measured ripple. The details of these predictions and additional ripple measurements are found in [X].

Summary

This section showed that the Dickson topology was a good match for the target power density and high efficiency requirement. With this topology, the η_{max} was 82 % with an ULE load power. For a 1/3 topology, this produced a high EEF of 64 %. The high efficiency and EEF are due to minimal control circuitry, thin-oxide transistors, a low input voltage, and the optimization of the SCN using methods in [22]. The converter was simulated and measured in an open-loop configuration. It was not possible to measure the efficiency due to an unknown error. However, the converter did function correctly when supplying a 32-bit adaptive processor. The performance of the Dickson DC-DC converter is summarized in Table 3.1. An improved Dickson converter design, which is built in 28 nm UTBB FD-SOI CMOS, is presented in the next section.

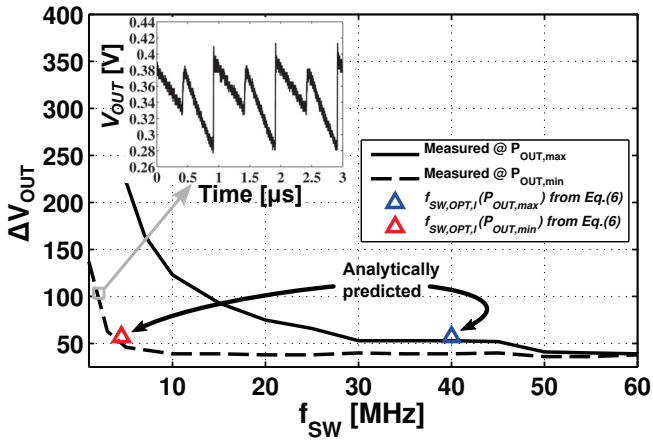


Figure 3.5. Measured and analytically predicted ripple of the 3:1 Dickson converter from [X]. ©2015 IEEE.

Table 3.1. Performance summary of the 3:1 Dickson converter.

	Value
Technology	28nm CMOS
Topology	step-down SC
C_{fly}	160pF (MOM)
C_{OUT}	200pF (MOM/MOS)
iVCR	1/3
Tested Input / Output Voltage	1-1.7V / (0.304-0.470V)
$f_{dc\text{-}dc,max}$	32 MHz
Load Range	14µW-115µW
Load Range in Ratio	1:8
Efficiency max	[1]82%@0.350V
EEF_{max}	[1]64%@0.350V
Efficiency (η) @ Sub-/Near-V_{th}	[1]75%@0.350V
Power Density @ η (mW/mm^2)	1.66@0.350V

[1]From simulations.

3.2 SC DC-DC Converters in UTBB FD-SOI

3.2.1 UTBB FD-SOI Background

UTBB FD-SOI CMOS has a number of advantages over traditional CMOS. For example, UTBB FD-SOI has improved SCE immunity, improved variability, latch-up immunity, and extended body-biasing (*a.k.a.* back-gate biasing) [44]. Back-gate biasing is more effective in changing a transistor's threshold voltage (V_{th}) than in advanced bulk CMOS for two reasons [45]. First, the range of bias voltages is larger since the bulk node is isolated from the drain and source. Second, the body-bias factor (γ) is higher. For example, at the 28 nm node, in UTBB FD-SOI $\gamma \approx 85$ mV/V while in bulk CMOS $\gamma \approx 25$ mV/V [46].

The application of back-gate bias, is useful in increasing transistor conductance with FBB [46–48] or decreasing leakage with reverse body bias (RBB) [45]. For SC DC-DC converters, increasing the conductance with FBB is beneficial since it allows for larger load power (*i.e.* large $P_{OUT,max}$). Similarly, RBB can be used to reduce leakage energy. Tradeoffs in performance and leakage due to back-gate biasing are key benefits of the UTBB FD-SOI technology.

With UTBB FD-SOI, RBB and FBB can be applied to regular threshold voltage (RVT) and low threshold voltage (LVT) transistors, respectively. As shown in Fig. 3.7, RVT transistors are implemented in a conventional well, where NMOS and PMOS transistors are above p- and n-wells, respectively. An FBB up to 0.6 V and RBB down to -3 V can be used with RVT transistors. The design in section 3.2.2 uses only RVT devices; RBB was applied to reduce leakage at low (nW) load power levels. As shown in Fig. 3.7, LVT transistors are implemented as "flip-well" transistors in which the NMOS and PMOS transistors are above the n- and p-wells, respectively. FBB up to 3 V and RBB down to -0.3 V is allowed. The design in section 3.2.3 uses only LVT devices; FBB was utilized to increase the maximum load-handling capability.

The generation of the back-gate bias voltage requires additional circuitry. Details of this circuitry lies outside the scope of this thesis. However, the designs presented in the following sub-sections both give measurement results with biasing schemes that have little or no impact on performance. Self-biasing techniques [49] and simpler single-well biasing techniques [50] will be explored in future implementations.

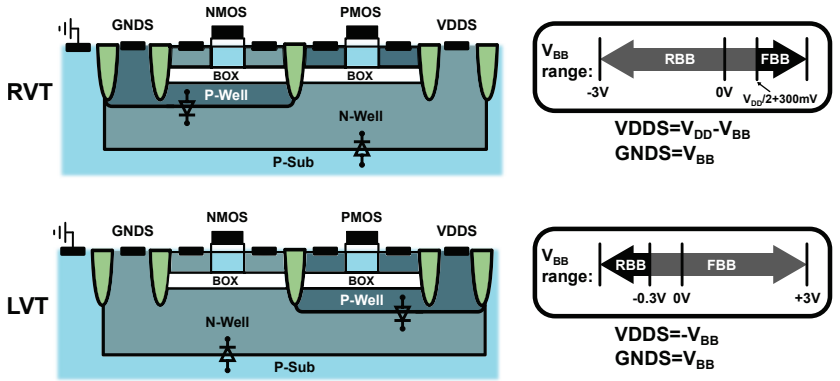


Figure 3.6. UTBB FD-SOI RVT and LVT transistors. The RVT and LVT transistors can realize performance advantages from the application of RBB and FBB, respectively [45].

3.2.2 3:1 Dickson DC-DC Converter

Introduction

The goal of the 3:1 Dickson DC-DC converter is to provide an efficient conversion from a 1.55 V prototype battery to an NT processor load. During 95% of the battery's discharge time, the voltage is between 1.5 V and 1.6 V, and thus, 1.5 V - 1.6 V is the main input voltage testing criteria. Due to the battery characteristics, and due to the fact that the NT processor load has a flat energy profile from V_{OUT}=0.35 V to 0.45 V, a single 1/3 topology is sufficient for this design.

Besides providing high efficiency under active load conditions, the DC-DC converter also should be efficient for sleep mode load conditions. As previously mentioned, toggling between a processor's sleep and active mode can produce large changes in load power [51]. Although the intended processor load only has an active mode, future implementations of the processor will have a sleep mode. Achieving high efficiency at nW loads (in sleep mode) is challenging due to control circuitry leakage energy losses [7, 19]. We explore the application of back-gate biasing to reduce control circuitry losses and increase efficiency for sleep mode. In UTBB FD-SOI, back-gate biasing can be applied to RVT transistors to achieve significant reductions in leakage [45].

Circuitry

The 3:1 Dickson DC-DC converter is shown in Fig. 3.7 (a). The core and control circuitry are designed to (efficiently) deliver an NT output voltage. The DC-DC converter's area of 0.023 mm^2 is mainly consumed by

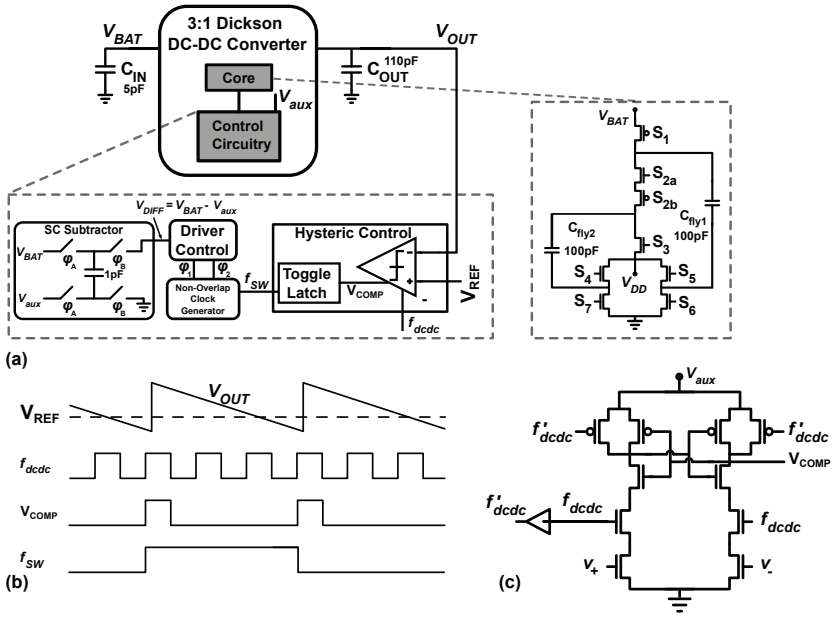


Figure 3.7. (a) Implementation of the 3:1 FD-SOI Dickson converter from [VIII]. The Driver Control is similar to the previous Dickson implementation (section 3.1). (b) Single Boundary control. (c) Clocked comparator.

the MIM capacitors $C_{fly1,2}$ within the core and output decoupling capacitance C_{OUT}.

The core and control circuitry of the converter use only thin-oxide RVT transistors. Multi-phase interleaving is not used since it adds large control circuitry losses at sleep mode load power levels. The core uses the same (Dickson) topology, and a similar driver control, as in the previous DC-DC converter in section 3.1. The core's switches are driven by tapered buffers [40, pp. 344-345]. Within the control circuitry, an intermediate rail generator (for V_{DIFF}) and hysteric control circuitry are used. The intermediate rail generator, which is an SC subtractor circuit, produces V_{DIFF}=V_{BAT}-V_{1V} for switches S_1 and $S_{2a,b}$. The SC subtractor circuit uses f_{dcdc} for its switching frequency. This switching frequency should be as low as possible to reduce power losses associated with switching the subtractor circuit (see Fig. 3.11).

The Hysteric Control block (Fig. 3.7) is used to regulate the DC-DC converter's output voltage V_{OUT}. This block uses discrete time hysteric control, which is an all-digital pulse frequency modulation (PFM) technique used to scale the DC-DC converter's switching frequency with power. Although most modern DC-DC converters use PFM, benefits have also been shown with digital capacitance modulation [52]. The Hysteric Control

block consists of a clocked comparator and an edge-triggered (toggled) latch to enable Single Boundary control [41] as shown in Fig. 3.7 (b). The clocked comparator drives V_{COMP} high if $V_{OUT} < V_{REF}$ and vice-versa. The Toggle Latch changes state every time the comparator detects a boundary violation. Thus, the actual switching frequency of the DC-DC converter is f_{SW}. The comparison and (latch) reset is done on the rising and falling edge of CLK, respectively.

The comparator is a key component of the Hysteric Control block. For this design, a low power clocked comparator is used as shown in Fig. 3.7 (c). Low NT input voltages (V_{REF},V_{OUT}) and a wide input frequency range (f_{dcdc}=50 kHz – 50 MHz) require careful design of the comparator especially at low frequencies. The comparator architecture is similar to [41] but with two different features. First, a delayed clock signal is added to the PMOS used for the latch reset. This delay in the latch reset ensures that the CLK is above V_t before the comparison is made, and thus, that variations in I_{DSx} are minimized. Second, all the transistor lengths were sized 4 x L_{min} to minimize (drain-source) leakage and ensure proper operation down to kHz input frequencies.

Measurement Results

The DC-DC converter was measured with different load powers, input voltages, output voltages, and temperature. The temperature results are discussed later in chapter 5 (subsection 5.3.3) whereas the performance under different load powers, V_{BAT}, and V_{OUT} is discussed as follows. The measured efficiency at NT voltages is shown in Fig. 3.8. The ULP mode uses a back-gate bias of $VBBP$=1.55 V/$VBBN$=-1.55 V while LP mode uses a back-gate bias of $VBBP$=0 V/$VBBN$=0 V. At V_{OUT}=0.465 V, the minimum efficiency was 71% for 104 nW to 140 μW loads. The peak efficiency over this load power range was 81%. At V_{BAT}=1.5 V and V_{BAT}=1.6 V, the peak efficiency was 81.4% and 80.1%, respectively (Fig. 3.8 (b)). Overall, the converter has high efficiency across a wide load power range.

The wide load power range is largely due to back-gate biasing. At sleep mode power levels, the DC-DC converter is able to increase its efficiency through increased RBB as shown in the measurement results in Fig. 3.10 (a). By applying RBB (with $VBBP$=2V and $VBBN$=-2V) at P_{OUT}=0.6 μW, the percentage of leakage power is reduced from 15.6% to 0.6%. Increasing RBB at higher load powers (*e.g.* P_{OUT}=10.6 μW), has minimal effects since leakage power is small relative to converter's power loss P_{loss} (as

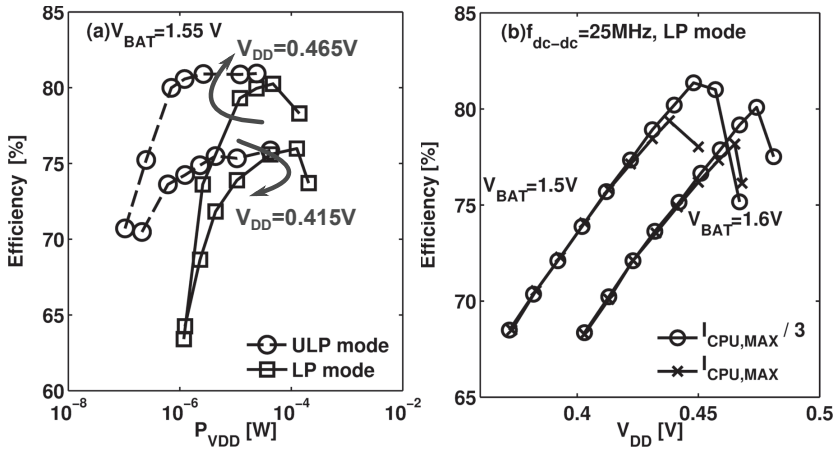


Figure 3.8. Measured converter efficiency. The ULP mode uses a back-gate bias of $VBBP$=1.55 V/$VBBN$=-1.55 V and LP mode uses a back-gate bias of $VBBP$=0 V/$VBBN$=0 V [VIII]. ©2015 IEEE.

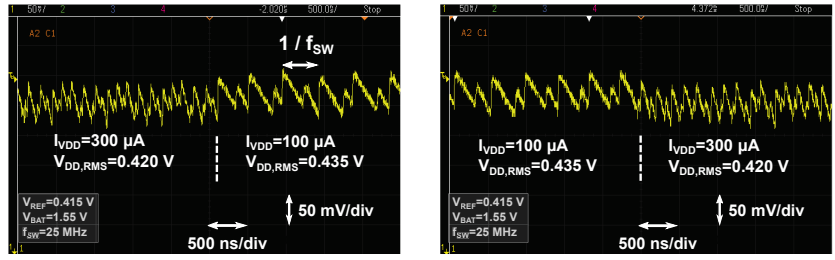


Figure 3.9. Effect of a load step on the 3:1 Dickson DC-DC converter.

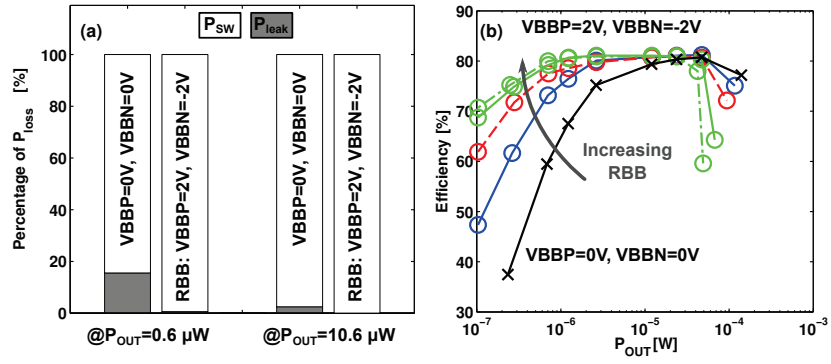


Figure 3.10. Measured characteristics of RBB.

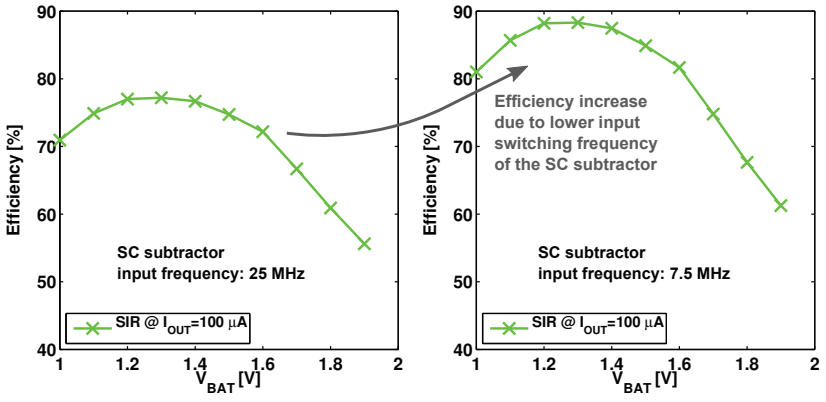


Figure 3.11. (a) Measurements of the DC-DC converter with the SC subtractor input frequency of 25 MHz and (b) 7.5 MHz.

shown in (2.4)). The effect of RBB on efficiency is shown in Fig. 3.10 (b). Overall, RBB has greater impact as the P_{OUT} is reduced. The reason is that the leakage power due to control circuitry losses (P_{cont}) increases as a percentage of P_{loss} as P_{OUT} decreases; this was also confirmed in [II].

When switching between different load powers, the DC-DC converter should still perform correctly. As shown in Fig. 3.9, the converter was measured with load steps and a fixed input frequency (f_{dcdc}) of 25 MHz. Load current steps between 100 μA and 300 μA are applied to model the processor's (load) characteristics. There is a clear change in the actual switching frequency (f_{SW}) of the converter when changing between load levels. As predicted by [41], hysteric control is a fast and stable control method. The $V_{OUT,RMS}$ is slightly larger than V_{REF} mainly due to the ripple [41]. However, the processor's input capacitance of 75 pF reduces $V_{OUT,RMS}$ to $\approx$ 0.415 mV under typical operation.

During measurement of the DC-DC converter, it was realized that the SC subtractor input frequency could have been reduced to improve efficiency. By re-configuring the SC subtractor to switch with f_{SW}=7.5 MHz rather than with f_{dcdc}=25 MHz, the efficiency of the DC-DC converter can be improved. As shown in Fig. 3.11, by reducing the switching frequency of the SC subtractor, the average efficiency was improved from 70.7 % to 80.1 %. Note that the DC-DC converter used SIR - a technique discussed later in chapter 5.

Table 3.2. Performance summary of the 3:1 Dickson converter.

	Value
Technology	28nm UTBB FD-SOI (RVT)
Topology	step-down SC
C_{fly}	200pF (MIM)
C_{OUT}	110pF
iVCR	1/3
Tested Input / Output Voltage	1-1.9V / (0.290-0.543V)
$f_{dc\text{-}dc,max}$	38 MHz
Load Range	209nW-205µW
Load Range Min. Efficiency (η_{MIN})	η_{MIN}=71%
Load Range in Ratio	1:981
Efficiency max	[1]81%@0.465V [1]76%@0.415V
EEF_{max}	[1]65%@0.415V
Efficiency (η) @ Sub-/Near-V_{th}	[1]76%@0.415V
Power Density @ η (mW/mm²)	5.5@0.415V

[1]V_{BATT}=1.55V and NBB (GNDS=VDDS=0V)

Summary

A fully integrated SC DC-DC converter was presented (Fig. 3.2). While connected to a Li-ion battery input, the DC-DC converter achieved a peak efficiency of 81% and was able to achieve efficiency over 71% for 104 nW to 140 μW loads. Back-gate biasing was used to reduce leakage power at sub-5 μW loads. A single topology allowed for high efficiency across a wide power range. Adding additional topologies was unnecessary and would have only increased complexity and losses.

3.2.3 2:1 Self-Oscillating DC-DC Converter

Introduction

The goal of the 2:1 self-oscillating DC-DC Converter is to achieve high efficiency over a wide load range. The motivation for the wide load range is to account for active and sleep modes in current ULE processors. A new (self-oscillating) topology is implemented and back-gate biasing is utilized to further improve its performance. More specifically, back-gate biasing is used to increase the maximum drive strength of switches in the SCN and to increase the switching frequency. This is useful when operating during a processor's active mode. The self-oscillating topology also works well at low (sleep mode) load power levels due to its minimal control circuitry [53].

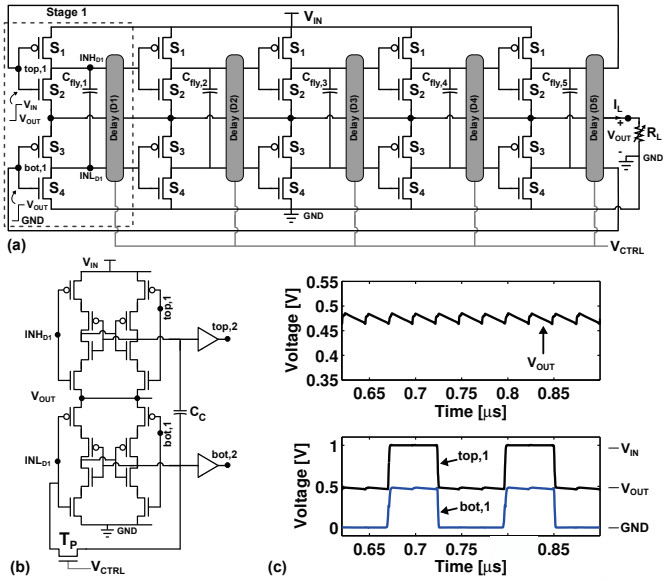


Figure 3.12. Implementation of the 2:1 self-oscillating converter from [VII]. (a) Schematic of the self-oscillating 2:1 DC-DC converter. $Cfly_{1-5}$ are each a 27 pF MIM capacitor. (b) Delay block Di. (c) Simulated results of V_{OUT} and voltages (top,1/bot,1) from Stage 1. ©2015 IEEE.

Circuitry

The self-oscillating 2:1 DC-DC converter is shown in Fig. 3.12 (a). The converter is comprised of two stacked ring oscillators. Clock generation and level conversion are inherent within the topology. During oscillation, each stage alternates its configuration in the same way as a conventional 2:1 converter. For example, in Stage 1, S_1 and S_3 turn *ON* at the same time in order to charge $C_{fly,1}$ while S_2 and S_4 turn *ON* at the same time during a discharge phase.

The self-oscillating converter is interleaved since each stage delivers charge at different phase times. Each of the five stages consists of three main blocks: a 27 pF MIM capacitor, charge transfer switches ($S_1 - S_4$), and a delay cell (D*i*). The LVT charge transfer switches form inverters that are approximately 2x larger than the largest design kit library inverter. The lengths of these inverters are sized 2x the minimum length to ensure that the leakage does not affect functionality at nW load power [54].

The variable delay cells (D1-D5) within each stage are used to adjust the switching frequency (f_{SW}) with changes in the load power ($P_{OUT} = V_{OUT} * I_L$). As shown in Fig. 3.12 (b), an individual delay cell consists of two leakage-based delay elements, a pass transistor (T_P), and a 0.2 pF

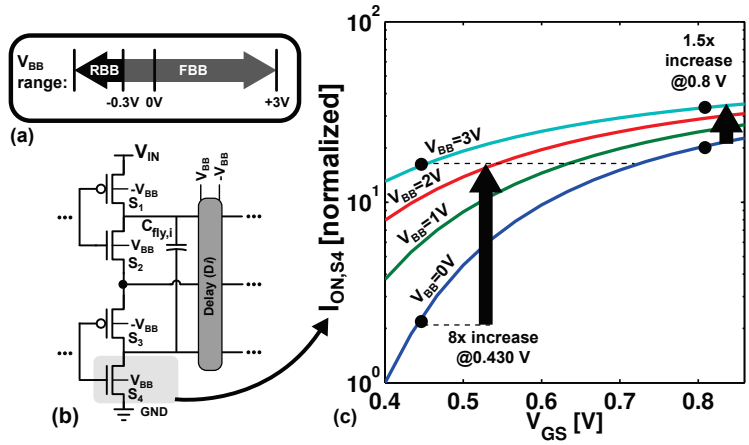


Figure 3.13. (a) V_{BB} range for LVT transistors [46]. (b) Back-gate bias connections in the converter. Within Di, the NMOS and PMOS have V_{BB} and -V_{BB} voltages, respectively. (c) Simulated change in $I_{ON,S4}$ due to V_{BB}. ©2015 IEEE.

MIM coupling capacitor labeled C_C. C_C ensures synchronization of the stacked ring oscillators. Additional details of the leakage-based delay an be found in [7, 55]. V_{CTRL} is used to adjust the amount of leakage within the leakage-based delay elements, and thus, adjust the delay (D*i*) between each stage. Circuitry required to enable closed-loop control of V_{CTRL} has minimal impact on conversion efficiency even at 1.7 nW load power [55].

The back-gate biasing scheme for the proposed self-oscillating converter is shown in Fig. 3.13. The biasing scheme was chosen to allow for bias voltages to be generated without sacrificing the efficiency of the converter. For example, V_{BB} (*e.g.* 1 V) can be generated from V_{IN} and -V_{BB} (*e.g.* -1 V) can be generated from a nW reverse body bias generator [56], respectively. The application of back-gate biasing on a single switch (*i.e.* S_4) in triode mode are shown in Fig. 3.13 (c). As V_{gs} approaches NT voltages, the gain in the drive strength of S_4 due to back-gate biasing becomes much more significant than at super-threshold voltages. Since the V_{gs} of all switches in the self-oscillating topology operate with NT voltages (assuming V_{IN}=1 V - 1.2 V), there is strong motivation to apply back-gate biasing.

The effect of back-gate biasing on all switches within the proposed DC-DC converter (Fig. 3.12) is found by examining the DC-DC converter's output impedance R_o (see (2.3)). To construct an equation for R_o that accounts for back-gate biasing, the G_{tot} is needed (in order to calculate R_{FSL}). From [VII], G_{tot} can be described by

$$G_{tot} = k(\frac{W_i}{L_i}\sum_{i=1}^{m} K_i(V_{GSi} - V_{th,i})) \tag{3.1}$$

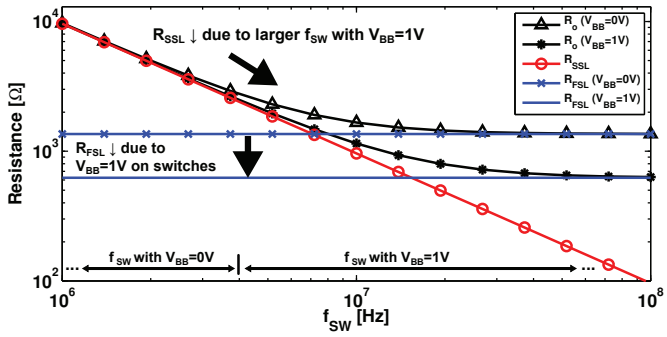


Figure 3.14. Analytical prediction of R_o from (2.3) with K_c=1/4, K_s=4, C_{tot}=135 pF, and G_{tot} from (3.2) [VII]. ©2015 IEEE.

where m is the number of switches in a stage, k is the number of interleaved stages, L_i and W_i are the common switch size parameters, K_i is the technology constant, and V_{GSi} is the voltage applied when the switch is *ON* (and in triode mode). Note that by decreasing the $V_{th,i}$ with increasing V_{BB} results in a larger overdrive voltage, and thus, a larger G_{tot}. By applying back-gate biasing with the biasing scheme from Fig. 3.13 (b), (3.1) expands to

$$G_{tot} = 5\Big\{(K_n\frac{W_n}{L_n}(V_{IN}-2V_{thn}+\gamma_n(2V_{BB}-V_{OUT}) \\ +(K_p\frac{W_p}{L_p}(-V_{IN}-2V_{thp}+\gamma_p(-2V_{BB}-V_{IN}-V_{OUT})\Big\} \tag{3.2}$$

Now that G_{tot} is known, R_o (from (2.3)) is plotted as shown in Fig. 3.14. The frequency range shown is for higher load powers (above 5 μW); the range of f_{SW} is estimated from simulations. The application of back-gate biasing has two important effects on the converter. First, a larger V_{BB} increases f_{SW} by decreasing the delay of both the inverter pairs (S_1/S_2 and S_3/S_4) and the delay cells. Thus, the f_{SW} range is shifted to higher frequencies for a given V_{CTRL} range. As a result, the R_{SSL} decreases. Secondly, a larger V_{BB} increases the overdrive voltage of the converter, and thus, decreases the R_{FSL}. The decreases in both R_{SSL} and R_{FSL} give a lower R_o, and thus, higher maximum power ($P_{OUT,max}$) since $P_{OUT}\alpha$ 1/R_o.

Measurement Results

The DC-DC converter's efficiency was measured at V_{OUT}=430 mV and 460 mV for nW to μW loads as shown in Fig. 3.15 (a). Back-gate biasing was applied for both V_{OUT}. The V_{CTRL} was adjusted over the same power range as in Fig. 3.15 (a) for V_{OUT}=430 mV. With V_{BB}=0 V, the V_{CTRL} (markers A and B), provides low f_{SW} to meet low power loads as shown

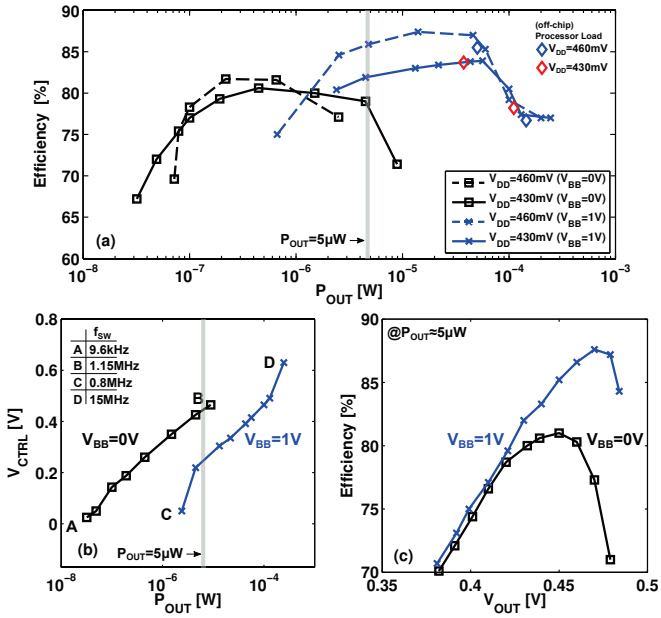


Figure 3.15. Measurement results of the proposed converter with back-gate biasing [VII]. (a) Efficiency vs. load power (P_{OUT}) at V_{OUT}=430 mV and 460 mV. (b) V_{CTRL} at V_{OUT}=430 mV; (c) Efficiency at P_{OUT} ≈5 μW. ©2015 IEEE.

in Fig. 3.15 (b). Increasing the back-gate biasing to V_{BB}=1 V gives higher f_{SW} over a similar V_{CTRL} voltage range. For a load power over ≈5 μW it is essential to use back-gate biasing of at least V_{BB}=1 V in order to maintain sufficient f_{SW} and switch conductance. Using back-gate biasing, the self-oscillating converter achieved a minimum efficiency of 75 % for 79 nW to 200 μW loads and a peak efficiency of 87 %.

The maximum load power of the self-oscillating converter was further increased by applying V_{BB} up to 3 V as shown in Fig. 3.16. The V_{CTRL} was a constant 0.7 V to ensure the maximum f_{SW} at each V_{BB} and the back-gate bias configuration was the same as in Fig. 3.13 (b). V_{BB} was

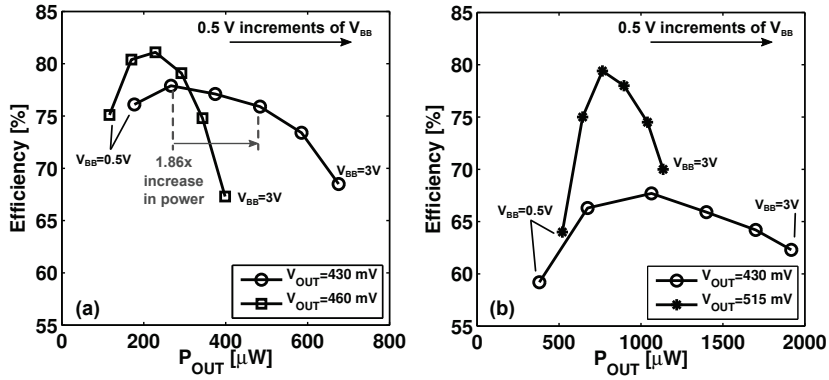


Figure 3.16. Measured effeciency at (a)V_{IN}=1 V and (b)V_{IN}=1.2 V [VII]. ©2015 IEEE.

swept from 0.5 V to 3 V in 0.5 V steps. The load power as a function of efficiency for V_{IN}= 1.0 V is shown in Fig. 3.16 (a). The measured increase in load power from V_{BB}= 1 V to 2 V was 1.86 x. Assuming FSL operation (*i.e.* $R_{SSL} \approx 0$), then an increase in load power requires a proportional decrease in R_o. Under this assumption, R_o decreases by 1.6 x in (2.3) when changing from V_{BB}=1 V to 2 V. The load power as a function of efficiency for V_{IN}= 1.2 V is shown in Fig. 3.16 (b). Higher P_{OUT} is possible due to the larger overdrive voltages (i.e. switches have larger V_{gs}).

Summary

A fully integrated SC DC-DC converter was presented (Fig. 3.12). The DC-DC converter achieved a peak efficiency of 87 % and was able to achieve efficiency over 75 % for 79 nW to 200 μW loads. Back-gate biasing was used to increase both the switch conductance and switching frequency at large loads. The self-oscillating topology proved to be advantageous at sleep power levels due to its minimum control circuitry. Since the converter is built from stacked ring oscillators containing inverters, full synthesis of this design is possible.

An additional back-gate biasing scheme could be beneficial for the self-oscillating DC-DC converter presented. Instead of requiring two separate back-gate bias voltages as previously shown, the DC-DC converter could have used a gate-bulk connection, or DTMOS [57], on all the switches. This may slightly decrease efficiency at active mode power levels due to increased gate capacitance, but efficiency would be slightly improved in the sleep mode power level (since no additional bias circuitry would be required). Additionally, switching between different bias schemes would be fast. For systems in which sleep mode power is dominant, the gate-bulk back-gate biasing scheme would be worthwhile to examine.

3.3 Implementation Summary

Three fully integrated DC-DC converters with an NT output voltage were presented. The first DC-DC converter, which was a 3:1 Dickson DC-DC converter, showed the benefits of the Dickson topology. Next, an improved 3:1 Dickson DC-DC converter was shown to provide efficient conversion over a wide load range from a 1.55 V Li-ion battery. This DC-DC converter made use of back-gate biasing to improve the load power range. Finally, a 2:1 self-oscillating DC-DC converter was given. This DC-DC converter,

Table 3.3. Performance summary of the 2:1 self-oscillating converter.

	Value
Technology	28nm UTBB FD-SOI (LVT)
Topology	self-oscillating step-down SC
C_{fly}	135pF (MIM)
C_{OUT}	0pF
iVCR	1/2
Tested Input / Output Voltage	1-1.2V / (0.380 - 0.485V)
$f_{SW,max}$	15 MHz
Load Range	79nW-200µW
Load Range Min. Efficiency (η_{MIN})	η_{MIN}=75%
Load Range in Ratio	1:2532
Efficiency peak	[1]87%@0.46V
EEF_{max}	[1]47%@0.460V
Efficiency (η) @ Sub-/Near-V_{th}	[1]75%@0.515V [1]77%@0.46V [1]77%@0.43V
Power Density @ η (mW/mm²)	62@0.515V 19.2@0.46V 24@0.43V

[1] V_{BATT}=1V and V_{BB}=1V

which also utilized back-gate biasing, had a self-startup capability, high conversion efficiency, and a wide load range. The performance of the three converters is later compared to state-of-the-art SC converters in Table 6.1 (chapter 6). Each of the converters are well suited for adaptive ULE loads. The next chapter examines the characteristics of adaptive ULE loads.

4. Adaptive Ultra-Low-Energy Processors

In order to design DC-DC converters for ULE adaptive processors, it is essential to understand the processor characteristics. This chapter presents the details of three ULE adaptive processor loads. Each processor operates at NT voltages and uses an adaptive timing scheme to save energy and operate reliably at ULV. The adaptive schemes are based on operating a system at a voltage and frequency point in which the timing of critical paths fails intermittently and are handled through detection and correction.

A brief overview of ULV operation is first given. Next, an introduction to an adaptive timing scheme, called timing-error detection (TED), is presented. The details of three implemented processors with TED (or similar schemes) are then given. Two of the processors were manufactured in 65 nm CMOS and one in 28 nm UTBB FD-SOI. The processor in subsection 4.3.2 iis the first-known TED processor able to operate in sub-threshold. The processor characteristics, which are most relevant to the DC-DC converter design, are highlighted throughout the chapter and summarized at the end. This chapter gives the most significant aspects of the original work. Additional details can be found in the related scientific publications: [IV], [VI], [I], and [VIII].

4.1 Overview

In order for ultra-portable electronics to operate with long lifetimes or even autonomously, systems must operate with ULE. These systems rely increasingly on low energy processing in order to reduce the (energy-dominant) wireless data transmission [58]. This increased focus on ULE processing has prompted an emerging class of processors that operate at or near the threshold voltage [9, 14, 15, 21, 46, 59]. These ultra-low-

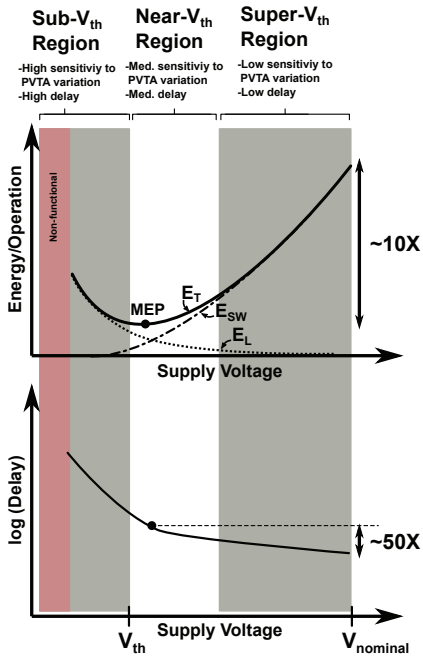


Figure 4.1. Energy per operation and delay as a function of supply voltage in modern CMOS.

voltages are where the minimum energy point (MEP) of modern digital systems is located. Operating at the MEP can bring energy savings around 10 x (Fig. 4.1). In general, the MEP is dependent on both the technology and architecture. Processors in older process nodes have a MEP within the sub-threshold region whereas newer CMOS processes have a MEP near the near-threshold region as shown in Fig. 4.1. As the leakage energy (E_L) increases for new processes, the MEP shifts right toward NT voltages [60].

The MEP is largely influenced by the delay. The propagation delay for an inverter operating in super-threshold is [61]:

$$t_d = \frac{KC_gV_{DD}}{(V_{DD} - V_{th})^{\alpha_v}}, \tag{4.1}$$

where K is a delay-fitting parameter, C_g is the output capacitance of a characteristic inverter, and α_v is the velocity saturation index [62]. In sub-threshold, the propagation delay of an inverter is [61]:

$$t_{d,sub} = \frac{KC_gV_{DD}}{I_o exp(\frac{V_{DD}-V_{th}}{nU_T})}. \tag{4.2}$$

where I_o is the ON current of the characteristic inverter, n is the sub-

threshold swing coefficient, and U_T is the thermodynamic voltage.

To better understand why the MEP is located at such low voltages, both the switching and leakage energy need to be examined. The energy losses due to short-circuit currents are negligible due to the exponential MOS I-V characteristics at ULV [60]. The switching energy (assuming rail-to-rail swing) is [61]:

$$E_{SW} = C_{eff}V_{DD}^2 = C_{TOT}\alpha V_{DD}^2, \tag{4.3}$$

where C_{eff} is the average effective switched capacitance, α is the activity factor, and C_{TOT} is the total physical capacitance. The leakage energy is [61]:

$$E_L = (I_{LEAK}V_{DD})T_{op} \tag{4.4}$$

$$= W_{eff}KC_gL_{DP}V_{DD}^2 exp(\frac{-V_{DD}}{nU_T}), \tag{4.5}$$

where T_{op} is the time to complete an operation and L_{DP} is the critical path depth in characteristic inverter delays. The total energy per operation is then expressed as:

$$E_T = E_{SW} + E_L \tag{4.6}$$

$$= V_{DD}^2[C_{eff} + W_{eff}KC_gL_{DP}exp(-V_{DD}/nU_T)]. \tag{4.7}$$

As shown in Fig. 4.1, the E_L dominants E_T due to leakage over large delay times within sub-threshold and near-threshold regions. Within the super-threshold region, the E_T is dominated by E_{SW}. The smallest energy for E_T is called the MEP. The V_{DD} location of the MEP, or $V_{DD,OPT}$, is of relevance for the DC-DC converter design. The $V_{DD,OPT}$ location is affected by changes in the activity factor (α) of a processor [60]. However, changes in the activity factor have a lesser impact on the MEP with scaling since C_{TOT} (from (4.3)) scales by 1/S (S>1). This behavior implies that the E_{SW} contribution reduces (moves to the right) and the flatness of the MEP increases for newer processes. In other words, uncertainty in V_{DD} has less of an impact on the MEP. The increasingly flat MEP region translates into an increasingly large operating voltage range with only a minimal penalty for operating outside the MEP. Therefore, the MEP region can be defined more generally as the region for which

$$E_{cy} - E_{cy,MEP} \leq x \cdot E_{cy,MEP} \tag{4.8}$$

where E_{cy} is the energy per cycle at V_{DD}, $E_{cy,MEP}$ is the energy per cycle at the MEP, and x is the per cent change from the MEP. As further discussed in [III], the MEP region increases with a decreasing α.

As the size of the MEP region continues to increase for new processes and for systems with a low to medium activity factor, it allows for innovative energy savings possibilities. Specifically, it can be utilized to remove the closed-loop MEP tracking control and achieve the energy savings with a simplified open-loop control. Further, the adaptive logic required to mitigate the MEP region variance effects allows for reduced design margins of the circuits associated with the logic. Here, the reduced susceptibility of the adaptive logic is used to relax the design constraints of the DC-DC converter.

Although there is decreasing motivation to precisely track the MEP, some MEP tracking systems have been shown to be useful. For example, the on-chip energy sensor in [16] is able to dynamically track the MEP of arbitrary digital circuits under different operating conditions. This sensor enables savings of 50 % to 100 %. This approach requires energy overhead (50 x larger than the energy of a 1-tap filter), and thus, it may need to be duty-cycled depending on the digital circuit power level.

When operating at the MEP, there are both performance and robustness limitations at low voltages for digital logic [60, 63]. The main reason for the performance limitation is that process, voltage, temperature, and ageing (PVTA) variations cause exponential changes in the current in the sub-threshold region as evident from (4.2). PVTA variations can be classified as either global (*e.g.* die-to-die, ageing, or temperature), or local (*e.g.* within-die, IR drops, jitter) [64]. The impact of variations requires large (speed) safety timing margins, which translates into higher energy consumption, to ensure robustness.

Process variations are of particular concern since they adversely affect the yield and may require (costly) individual post-fabrication measurements to ensure robustness at ultra-low-voltages. Process variations are due to die-to-die (lot-to-lot and wafer-to-wafer) variations and within-die variations (from factors such as nondeterministic placement of dopant atoms and variation in L) [60, 65]. Within-die variations have a large impact on the transistor's V_{th}. The sigma for V_{th} random doping fluctuations (RDF) is proportional to $(WL)^{-1/2}$ [61], and thus, sizing considerations are important in reducing performance limitations.

Besides the performance limitations, digital logic also has functional ro-

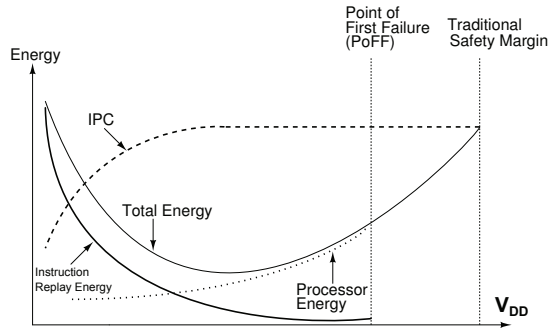


Figure 4.2. Relationships between output voltage (V_{DD}) and energy for a TED system with fixed operation frequency. As the error rate increases beyond the point of first failure (PoFF), the recovery energy grows due to the effort required in correcting the errors.

bustness limitations at sub-threshold voltages due to the previously described PVTA variations (see Fig. 4.1). The high impact of variability in the I_{ON}/I_{OFF} current ratio at such low voltages can lead to bad output logic levels [9, 60, 63, 65]. This behavior in turn leads to functional failures of subsequent gates as shown in [V].

To solve the performance and robustness limitations, adaptive methods are needed. In super-threshold, a popular solution for overcoming the need for large safety timing margins has been to use canary (replica) circuits. However, canary circuits can only compensate for PVTA variations that are global and slow-changing [64]. The fact that they cannot compensate for local variations (*e.g.* within-die), means that they are not suitable for sub- or near-threshold operation. To compensate for both global and local PVTA variations, timing-error detection (TED) is proposed in the next section.

4.2 Timing-Error Detection (TED)

TED is an adaptive method that has been shown to reduce PVTA variation-induced safety margins [64, 66–70], which are traditionally used across all corners to ensure a sufficient yield. The reduced safety margins with TED can be turned into power savings (*i.e.* lower V_{DD} [67]), or a higher yield [64]. As shown in Fig. 4.2, TED systems can scale the V_{DD} until the point-of-first-failure (PoFF). In other words, the system operates at a voltage/frequency point in which the timing of critical paths fails intermittently. The failed timing occurrences are detected and corrected, for example, with an instruction replay system. If the error rate is suffi-

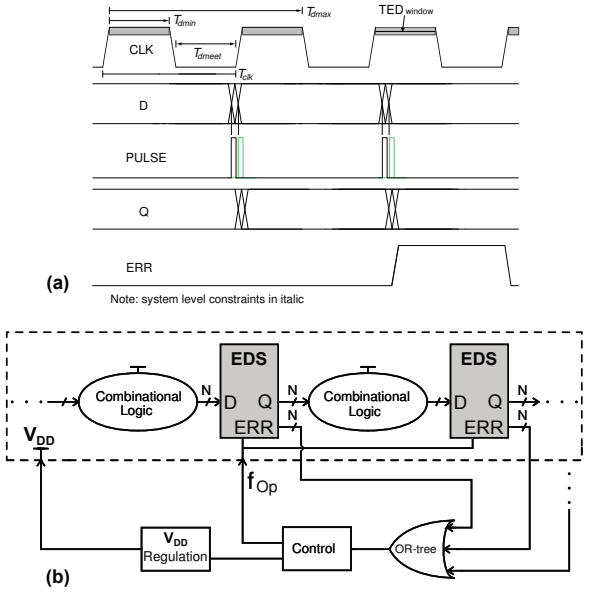


Figure 4.3. (a) TED operation with a dynamic node-style error-detection sequential (EDS) circuit. The transition-generated PULSE signal is used to change the state of a dynamic node and generate a timing error, or ERR. (b) Block diagram of a pipeline-based TED system.

ciently low (*e.g.* 0.04% in a study by Blaauw *et al.* [67]), then an energy consumption benefit is achieved as a result of operating at a lower voltage. The error rate must be kept low to ensure that the instruction replay portion of the TED system does not consume too much energy.

Important signals from a TED system are shown in Fig. 4.3 (a). To operate the TED system without timing errors, data (D) should transition after T_{dmin} and before the period of CLK (T_{clk}); this is called the T_{dmeet} region. If data would arrive before T_{dmin}, false errors would result. To meet this requirement, additional delay elements need to be added to any paths that violate T_{dmin}. The delay elements add power consumption overhead. Data transitions under the TED window are flagged as timing errors. Data transitions beyond T_{dmax} allow the system to miss timing errors. The timing constraints within a TED system can be summarized in terms of the duty cycle (d) and period (T_{clk}) of the CLK signal:

$$T_{dmin} = d * T_{clk} \tag{4.9}$$

$$T_{dmax} = (1 + d) * T_{clk} \tag{4.10}$$

The key component used to flag timing errors is called an error-detection sequential (EDS) circuit. EDS circuits generate error signals when the

path setup timing fails (*i.e.* if D transitions under the TED window). Within a TED system, the EDS circuits are placed at critical logic paths where timing errors can occur as shown in Fig. 4.3 (b). When timing errors are detected, the operation frequency (f_{Op}) or supply voltage (V_{DD}) can be adjusted to prevent data transitions at T_{dmax}, and thus, ensure operation without system failure. The TED window for the EDS circuits can be tied to the clock signal [67], or it can be generated independently [64].

There are two main types of EDS architecture: a dynamic node [67, 71, 72] and a delayed shadow latch [66, 73]. Of these architectures, the dynamic node can achieve a lower power and lower clock node capacitance. The dynamic node implementation typically uses an inverter delay chain and a logic gate (*e.g.* XOR), to produce a signal pulse. The signal pulse, or PULSE, as shown in Fig. 4.3 (b), is used to flip the state of a dynamic node and generate a timing error signal. The inverters and logic gates used to produce the PULSE signal require a high level of precision across all PVTA variations, especially at sub- and near-threshold voltage levels. In addition to being robust to PVTA, the size of the PULSE should be minimized since it limits the speed of the entire TED system. Designing the inverters and gates that generate the PULSE signal is one of the most challenging design tasks within the EDS circuit.

4.3 Implementations

4.3.1 Adder with TED

We designed and fabricated a TED system level test circuit in a 65 nm CMOS. The test circuit, which is referred to as SystemTest1 in Fig. 4.4 (a), is composed of two main parts: an adder and EDS circuits (called *TDTBsub1*). The EDS circuits are used to flag timing errors between the combinational logic (*i.e.* adder). Input data *D* is first serially loaded into the 60 input shift registers. The data is then passed to 60 (*TDTBsub1*) registers and then added together. The output of the adder is again placed through 60 *TDTBsub1* latches. From the *TDTBsub1* latches, the output is level-shifted (with levelS) and given to the output shift-registers (with shiftO).

The schematic of *TDTBsub1* is shown in Fig. 4.4 (b). It is a dynamic node style EDS and it is similar to the (super-threshold) EDS in [66],

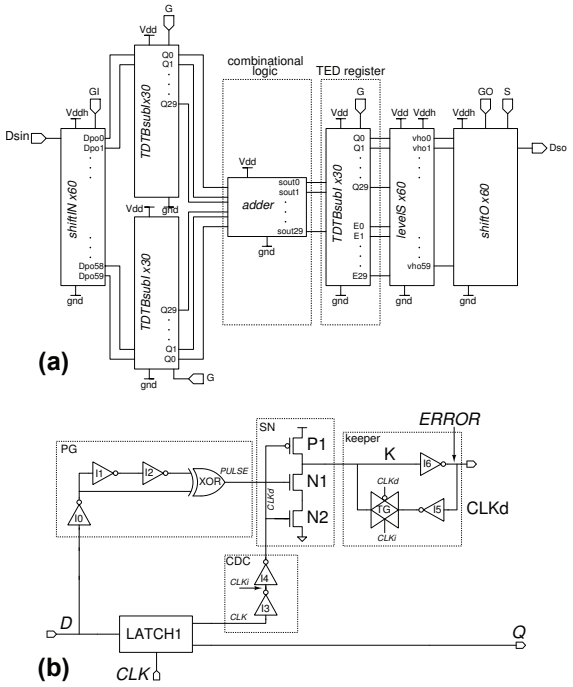


Figure 4.4. (a) SystemTest1 consists of an adder and an EDS circuit called *TDTBsub1*. (b) Circuit diagram of *TDTBsub1* [IV]. ©2009 IEEE.

except that it is designed to operate in sub-threshold. The operation of *TDTBsub1* is performed by a clock delay chain (CDC), a pulse generator (PG), a switching network (SN), and a keeper. The CDC provides signals for the transmission gate (TG). The PG provides a short voltage pulse signal called *PULSE* that occurs at each transition of *D*. If *D* transitions at the same time *CLK* is *HIGH*, the *PULSE* signal from PG allows the SN to pull node K low. As K is pulled low, the keeper switches states and *ERROR* is driven *HIGH*. During a reset of ERROR (at the negative edge of CLK), P1 is able to reliably drive K *HIGH* by breaking the keeper feedback with the TG [74]. All of *TDTBsub1*'s (HVT) transistor widths were up-sized according to the sizing metric of [61]. To reduce leakage, the L of most transistors were sized as Long-Le transistors (*i.e.* nominal + 10%), since Long-Le transistors have three times lower leakage with only a 10 % reduction in speed [75].

Measurement results of SystemTest1 are shown in Fig. 4.5. As expected, reducing V_{DD} provides large reductions in energy per operation. If a DC-DC converter was to supply V_{DD}, there is an important observation that can be made from the TED system measurements. The energy per operation becomes less sensitive to variations in V_{DD} for sub- and near-

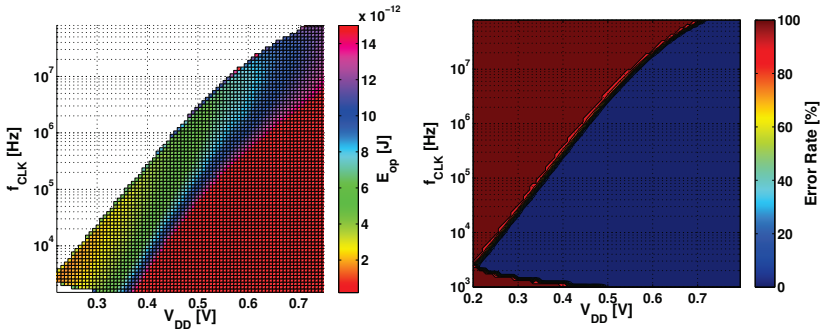


Figure 4.5. Energy per operation as a function of supply voltage (V_{DD}) and operation frequency (f_{op}); (b) Error rate (R) as a function of V_{DD} and f_{op}. As V_{DD} is reduced below 0.4 V, the error rate starts to increase for low f_{op} due to the leakage in N1 and N2 [IV]. ©2009 IEEE.

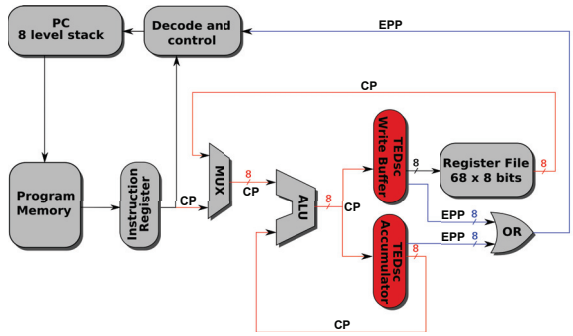


Figure 4.6. 8-bit sub-threshold processor with TED. The timing error signal propagation paths (EPP) are highlighted in blue and the critical paths (CP) in red [I]. ©2012 MDPI.

threshold regions. For example, the energy per operation increases 22.1 % and 33.3 % from 0.25 - 0.3 V and 0.3 - 0.35 V, respectively.

4.3.2 8-bit Processor with TED

To expand the previously described TED test system, an 8-bit processor was designed with TED (Fig. 4.6). The processor, which is described in [I], is capable of sub-threshold operation, has an 8-bit commercially-compatible core, and is built in 65 nm CMOS. It is the first-known TED processor able to operate in sub-threshold. The architecture of the CPU is an accumulator-based style in which the second operand is always the accumulator register. The processor has a three-stage pipeline that can generate timing errors from EDS circuits within the critical path. There is a total of 20 EDS circuits; eight of them are in the accumulator register, eight of them are in the register file write buffer, and four of them are used for the arithmetic and logic unit (ALU) flags.

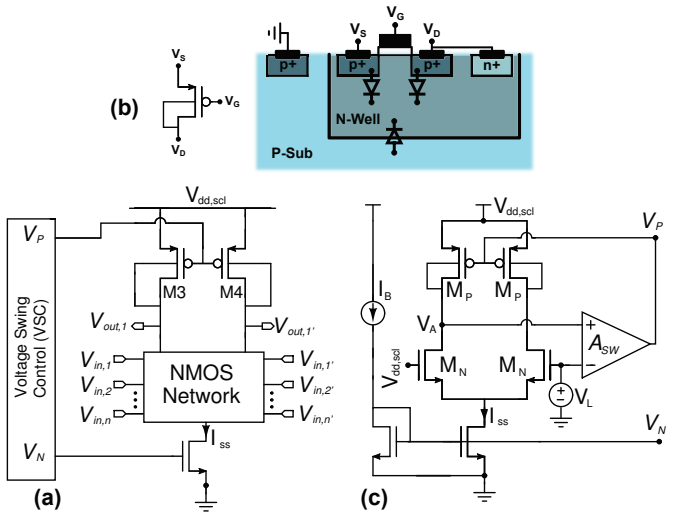


Figure 4.7. (a) Bulk to drain PMOS and cross section; (b) STSCL; (c) Voltage swing control (VSC).

The EDS circuit for the 8-bit processor uses sub-threshold source-coupled logic (STSCL) rather than traditional static CMOS. Depending on a ULE digital system's logic depth, leakage current, activity factor and operation frequency, STSCL can have advantages over static CMOS [76]. STSCL is targeted for ultra-low-power circuits which have relaxed speed requirements.

Similar to source-coupled logic (SCL) [77], an STSCL gate is composed of a network of differential NMOS pairs, adjustable PMOS loads (M_3,M_4) with output resistances of R_P, and an adjustable tail current I_{SS} as shown in Fig. 4.7 (a). The NMOS pairs are used to construct logic gates. I_{SS} and the PMOS loads are used to generate a proper voltage swing within the logic gates. The voltage swing is defined as V_{SW}=$|V_{out1} - V_{out1'}|$=R_P*I_{SS}. The bulk connection of the PMOS load is what differentiates SCL and STSCL. As shown in Fig. 4.7 (b), the bulk is connected to the drain (source) in STSCL (SCL). By connecting the bulk to the drain in STSCL, a more linear I_{DS}-V_{DS} characteristic is achieved [76, 78].

The bulk to drain connection does have one inherent limitation: the voltage swing is limited to 400-500 mV to ensure that the source to bulk diode does not become forward biased. However, in STSCL, the minimum voltage swing is well below this limitation. With low I_{SS}, the NMOS pairs operate in sub-threshold, and thus, require a minimum voltage swing as low as $4*n*U_T$, or $\approx$ 150 mV (at room temperature and n=1.5). The voltage swing is maintained over global variations by dynamically adjusting the size of the (PMOS load) R_P and the magnitude of I_{SS}.

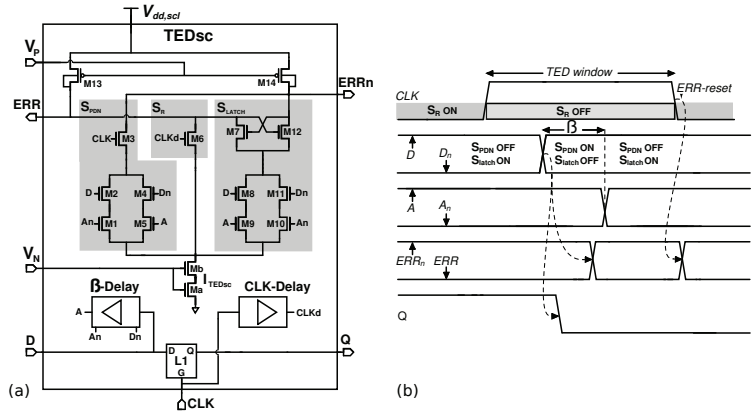
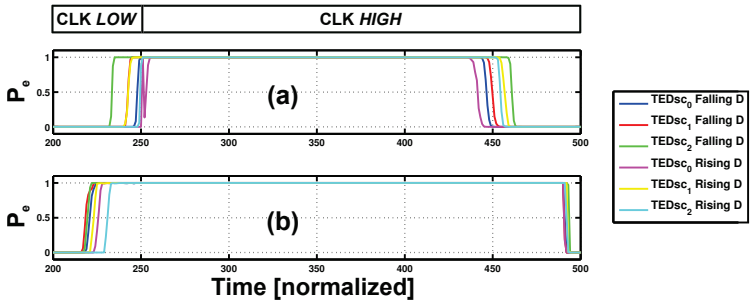


Figure 4.8. (a) TED_{sc} schematic; (b) TED_{sc} timing diagram.

The size of R_P and the magnitude of I_{SS} are both adjusted by the voltage swing control (VSC) block shown in Fig. 4.7 (c). The VSC decreases the dependence on global variations (*e.g.*, supply noise, temperature fluctuations, and ageing) by adjusting V_P through negative feedback. The bias voltage (V_P) from one VSC can be used for a large number of TED_{sc} gates [79]. The VSC for the EDS circuits is composed of a two-stage, Miller-compensated opamp (A_{SW}). The opamp is able to maintain an open-loop gain of 40 dB for all the global process corners (TT, FF, SS, SF, and FS). Simulations at -40°C to 90°C showed that the VSC generated a V_P to enable correct functionality of TED_{sc}.

The TED_{sc} schematic and timing diagram are shown in Fig. 4.8. TED_{sc} is able to detect timing errors when transitions of data D occur within the TED window. During a transition of D under a TED window, the pull-down network (S_{PDN}) receives signals from the β-Delay block to pull ERRn low, and consequently, to drive ERR high. After a delay (β), the new values of ERRn and ERR are latched until an error reset (ERR–reset) at the negative clock edge. The error reset is performed with the inverted clock signal CLKd that is applied to the reset pull-down block S_R.

TED_{sc} was measured within a test digital system consisting of three TED_{sc}s and combinational logic. The clock frequency of the digital system was fixed at 10.37 kHz. TED_{sc} and VSC used the following settings: $V_{dd,scl}$=400 mV and V_L=200 mV. Thus, V_{SW}=$V_{dd,scl}$-V_L=200 mV. With these settings, the probability of a timing error for the three TED_{sc}s was measured as a function of time as shown in Fig. 4.9. There was 500 points measured over one clock cycle. At each point there were 16384 (rising and falling) transitions.



Graph	V_{DD}	f_{CLK}	$t_{dD\text{-}ERR}$	I_{TEDsc}	TEDsc power
(a)	300 mV	10.37 kHz	~15 FO4	301 pA	150 pW
(b)	300 mV	10.37 kHz	~3 FO4	1.56 nA	655 pW

Figure 4.9. Measurements of TED_{sc} with ITEDsc of (a) 300 pA and (b) 1.5 nA.

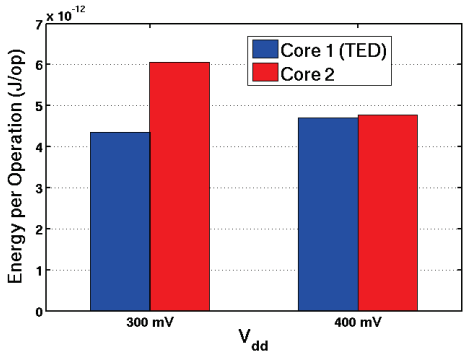


Figure 4.10. Energy per operation of Core 1 (with TED) and Core 2 (without TED). ©2012 MDPI.

Two bias currents were used in the measurement of Fig. 4.9. At the lower bias current of 300 pA (Fig. 4.9 (a)), the probability of a timing error is closer to the positive edge of CLK and farther from the negative edge CLK. This behavior is caused by two effects. First, a smaller bias current means that the time required for PULSE and CLK to be *HIGH* simultaneously is increased. Second, the effects of variation are more evident at the lower bias current since transistors within the NMOS network are deeper in sub-threshold. Recent techniques [80] could be applied in future implementations of TED_{sc} to reduce this variation. In summary, the power in TED_{sc} can be reduced by using lower bias currents with the tradeoff of increased variability.

To understand the benefits of using TED_{sc} in a digital system, a TED-enabled core (Core 1) and a non-TED core (Core 2) were designed in 65 nm CMOS. Core 1 used 20 TED_{sc}s. The energy per operation for both cores is shown in Fig. 4.10. At 300 mV, Core 1 (TED) uses 28% less energy per operation than Core 2. If Core 1 is supplied by a DC-DC converter,

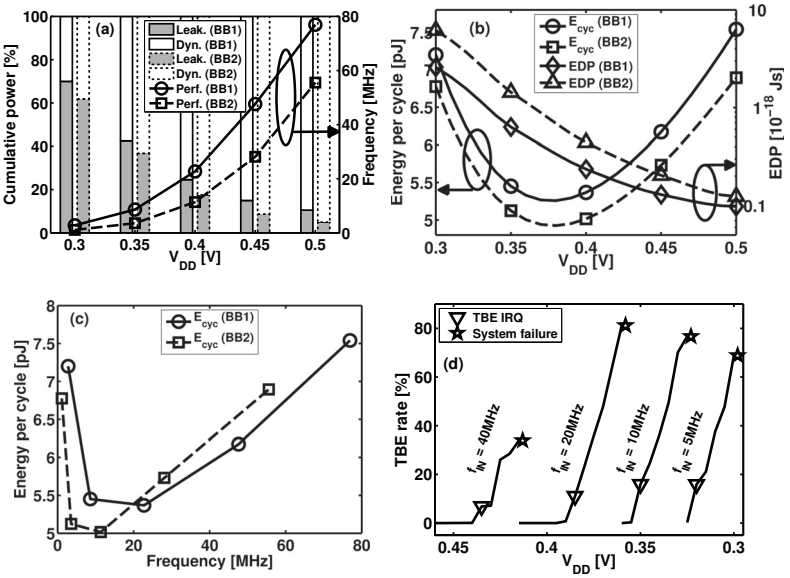


Figure 4.11. Measured processor characteristics [VIII]. ©2015 IEEE.

the flatness of the energy consumption between 300 mV and 400 mV for Core 1 implies relaxed constraints on ripple and regulation. Additional measurement details of the TED system can be found in [I] and [81].

4.3.3 32-bit Processor

Expanding on to the previous two TED systems, led to an improved adaptive processor capable of sub- and near-threshold operation. The processor is a customized 32-bit LatticeMicro RISC [82] with timing-error-prevention (TEP) in 28 nm UTBB FD-SOI. TEP is similar to TED in that it detects failed critical paths. However, TEP uses adaptive timing margining rather than instruction replay [9]. The author did not design the processor but did contribute to system measurements of the processor [VIII]. The goal of this subsection is to highlight the characteristics of the processor that affect the DC-DC converter design.

Measurements of the processor's power distribution, energy, performance, and energy-delay product (EDP) with two back-gate bias configurations (BB1, BB2) are shown in Fig. 4.11 (a)-(d). BB1 ($VBBP$=-0.5V,$VBBN$=0V) was used for enhanced performance while BB2 ($VBBP$=0V,$VBBN$=-0.5V) was used for low leakage. Larger back-gate bias voltages could have been applied, but the I/O pad limited the voltage to +/- 0.5 V.

With regards to DC-DC converters, there are three observations from the processor measurements in Fig. 4.11. First, even small changes in

back-gate bias generate large changes in the operation frequency, and thus, load power. Similar ULE processors in UTBB FD-SOI have shown large changes in performance and load power due to the strong effects of back-gate biasing at low voltages [83]. A DC-DC converter needs to operate efficiently over these load power changes. Second, the energy per operation is flat at sub- to near-threshold voltages (Fig. 4.11 (b)). Third, as shown in Fig. 4.11 (d), the regulation of V_{DD} is relaxed in terms of processor functionality. For example, if the processor is operating at 20 MHz and the DC-DC converter is supposed to regulate to V_{DD}=0.4 V, but the actual V_{DD} is 0.380 V, then the error rate is higher than expected. However, the inaccuracy in the regulation does not cause a system failure (since the TEP adaptive processor can handle high error rates). If the error rate is too high, and subsequently, causing too large energy consumption, then a closed-loop controller can use the measured error rate to adjust the operation speed (and/or V_{DD}) [64].

4.4 Summary

A brief overview of ULV operation was first given. The benefits and challenges associated within this region were explained. To achieve robustness and ULE at ultra-low-voltages, adaptive techniques such as TED can be used. An introduction to TED was presented to give the necessary background for three implemented TED processors. The first-known TED processor with sub-threshold operation was shown. Characteristics of ULE processors relevant to DC-DC converter design were highlighted throughout the chapter. The flatness in TED energy per operation curves near the MEP and adaptivity of the load allows for relaxed design constraints in the DC-DC converter. The next chapter focuses on designing a DC-DC converter/processor system.

5. Co-Design of DC-DC Converters and Adaptive Processors

The previous two chapters presented independent characteristics of DC-DC converters and ULE processors. The goal of this chapter is to identify the interdepedencies of the DC-DC converter and the ULE processor load. In other words, the chapter examines how these blocks operate together and present solutions to minimize the total system energy per operation.

The input voltage considerations for the DC-DC converter are presented first. These affect a number of different design choices for the DC-DC converter. The input voltage does influence the system energy per operation, and therefore, it is important to consider. Typically, DC-DC converters use a fixed input voltage (*e.g.* 1 V), or a battery for their input voltage. Two of the following DC-DC converters uses a fixed input while the final DC-DC converter use a prototype Li-ion 1.55 V battery input. The low and flat discharge characteristics of the prototype battery are well-suited for future ULE systems.

The DC-DC converter steps down the battery voltage and regulates to an NT output voltage. Both traditional and new regulation techniques for the DC-DC converter are given in this chapter. A new technique called SIR shows promising results for ULE processors. Next, system measurement results show how the choices in input voltage, DC-DC converter designs, and the ULE processor performance influence the system energy per operation. Measurements with the prototype 1.55 V Li-ion battery, a DC-DC converter, and a 32-bit adaptive processor show that ultra-low (system) energy is possible. Finally, a summary is given to highlight the most important considerations for DC-DC converter/ULE processor systems.

The most significant aspects of the original work are given in this chapter and additional details can be found in the related scientific publications [III], [IX], and [VIII].

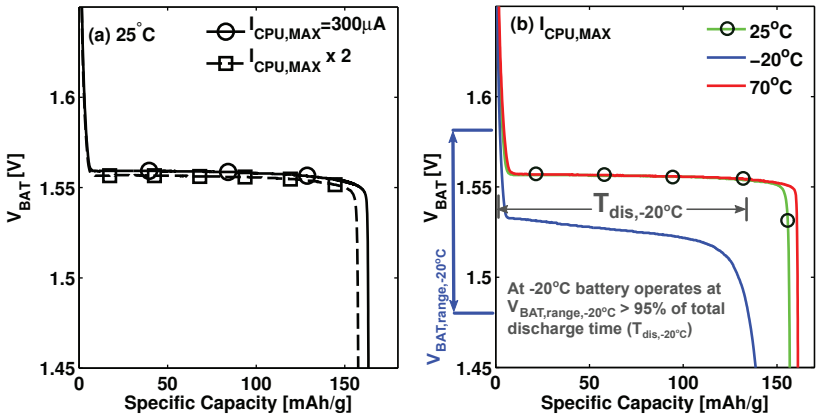


Figure 5.1. Measured discharge characteristics of the prototype 1.55 V Li-ion battery proposed in [36]. The battery has a flat discharge curve even with variations in load current (*i.e.* I_{CPU}), and temperature. This same battery is used as the input voltage to the DC-DC converter in section 5.3.3. ©2015 IEEE.

5.1 Input Voltage Considerations

The input voltage to the DC-DC converter affects the system energy consumption. First, the larger the range of discharge voltage, the more challenging it is to achieve high efficiency in the DC-DC converter since more topologies and control circuitry are required. Second, as discussed in chapter 2, a higher input voltage requires a lower VCR. Achieving high efficiency with a low VCR is not possible with SC DC-DC converters.

Many portable applications use a Li-ion batteries, which operate from 2.9 V - 4.2 V and nominally at 3.6 V. Traditional Li-ion batteries are an adequate solution for older portable electronics with 1 V supplies and larger breakdown voltages. But for future portable electronics that require near-threshold voltages (0.3 - 0.5 V) and have sub-1.1 V breakdown voltages, traditional Li-ion batteries are not a good solution. The VCR is too low to achieve high efficiency and the high nominal voltage may cause overstress on the DC-DC converter's switches [22]. To date, conversion from a traditional Li-ion down to a near-threshold voltage has not been shown.

Based on the previously mentioned challenges, there is strong motivation to use a battery that has similar (volumetric energy density) characteristics to the traditional Li-ion but operates with a lower nominal voltage. One such battery is the prototype 1.55 V Li-ion battery proposed in [36]. This battery also has the advantage of a flat discharge curve as shown in Fig. 5.1. We present measurements with this battery later in section 5.3.3.

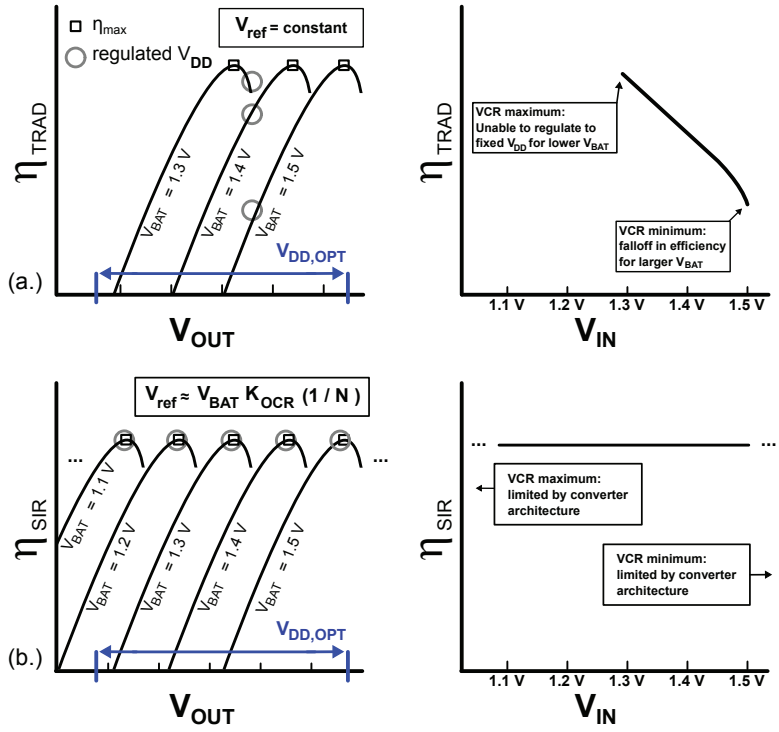


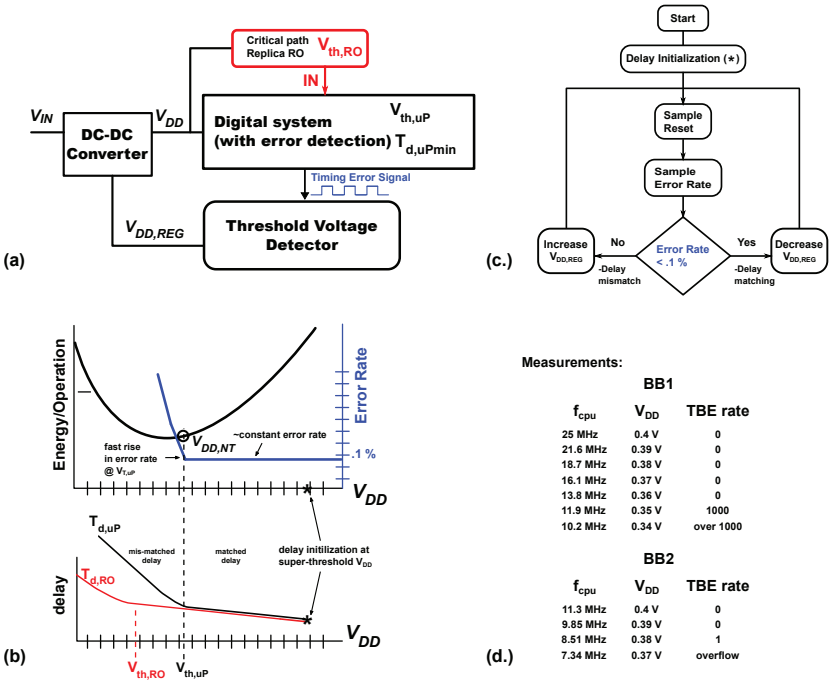
Figure 5.2. (a) Traditional and (b) scaled-input regulation techniques. ©2015 IEEE.

5.2 DC-DC Converter Regulation Techniques

Traditional Versus Scaled-Input Regulation (SIR)

For changes in the input voltage or load power, the DC-DC converter needs to regulate to the desired V_{OUT}. Traditional regulation for SC DC-DC converters require that the load has a fixed V_{OUT} (*i.e.* constant V_{ref} within the feedback circuitry) at each V_{IN} as shown in Fig. 5.2 (a), the peak conversion rate can only be reached at certain points of V_{IN}. Therefore, it is difficult to maintain high average efficiency for large changes in V_{IN}. In order to maintain high efficiency over a large range of V_{IN}, the V_{ref} can be adjusted linearly with V_{IN}. In other words, V_{OUT} scales linearly with changes in V_{IN} and the V_{OUT}/V_{IN} ratio is constant.

Allowing for a nearly constant V_{OUT}/V_{IN} for changing V_{IN} enables η_{max} to be achieved for a wide V_{IN} range. This scaling technique is called scaled input regulation (SIR). A conceptual diagram of the SIR technique is shown in Fig. 5.2 (b). The SIR technique has been shown to provide high efficiency across a large range of V_{IN} [III]. V_{ref} can be adjusted linearly with V_{Batt} using a resistor or diode voltage divider connections to V_{Batt} [84]. The benefits of the SIR technique are also discussed in [IX].



f_{cpu}	V_{DD}	TBE rate
25 MHz	0.4 V	0
21.6 MHz	0.39 V	0
18.7 MHz	0.38 V	0
16.1 MHz	0.37 V	0
13.8 MHz	0.36 V	0
11.9 MHz	0.35 V	1000
10.2 MHz	0.34 V	over 1000

BB2

f_{cpu}	V_{DD}	TBE rate
11.3 MHz	0.4 V	0
9.85 MHz	0.39 V	0
8.51 MHz	0.38 V	1
7.34 MHz	0.37 V	overflow

Figure 5.3. (a) Threshold voltage tracking loop within a digital CMOS system (b.) Conceptual diagram describing how the threshold voltage is found within the system. The key observation is that the threshold can be found by detecting a mismatch in $T_{d,RO}$ and $T_{d,uPmin}$. (c) Threshold voltage tracking loop flowchart. (d) Measurement results of the concept with a 32-bit (TEP) processor and an ideal voltage source.

Threshold Voltage Tracking Loop

The threshold voltage tracking loop is shown at the system-level in Fig. 5.3. It is composed of a digital system with timing-error prevention (TEP), a critical path replica RO, a threshold voltage detector, and a DC-DC converter. An important detail in this system is that the digital system and the critical path replica RO do not have the same threshold voltage (*i.e.* $V_{th,uP} \neq V_{th,RO}$). The goal of the tracking loop is to find the digital system's threshold voltage ($V_{th,\mu P}$). This goal is accomplished by identifying the V_{DD} at which the error rate rises above a (typical) rate of .1 % as explained below in more detail.

The first step in the tracking loop is the delay initialization. The delay of the critical path replica RO signal (IN) is tuned (by adding or removing RO stages) to match the minimum delay of the digital system. In other words, $T_{d,IN}$ = $T_{d,uPmin}$ after the delay initialization (even though the critical path replica RO and digital system have different threshold voltages). Note that the delay initialization is done at a super-threshold V_{DD}. The $T_{d,IN}$

and $T_{d,uPmin}$ have matched delay until $V_{DD} \approx V_{th,uP}$. At this point, the error rate rises quickly since the exponential delay change in $T_{d,uPmin}$ becomes effective. The V_{DD} at which the error rate rises beyond .1 % is the flagged as the location of the digital system's threshold voltage. Since the critical path replica RO has a lower threshold voltage than the digital system, the $T_{d,IN}$ still follows a quadratic change in delay (until $V_{DD} \approx V_{th,RO}$).

The threshold voltage tracking loop flowchart is shown in Fig. 5.3 (c). After a sample reset, there is a sampling time in which the error rate of the digital system is sampled. If the error rate is less than or equal to, for example .1%, the threshold voltage tracking loop lowers $V_{DD,REG}$. For V_{DD} above $V_{th,uP}$, a change in $V_{DD,REG}$ produces an (approximately) quadratic change in the critical path replica RO delay. The sample reset and sampling of the error rate resume. As this cycle continues, the $V_{DD,REG}$ will eventually reach $V_{th,uP}$. At this point, the error rate is greater than .1% and the threshold voltage of the digital system is detected.

The threshold voltage detector concept was confirmed with measurements of a 32-bit microprocessor and ideal voltage source. The results are shown in Fig. 5.3 (d). The frequency was reduced approximately quadractically until an error rate increase was observed. The point at which the error rate increases is (approximately) the threshold voltage ($V_{th,uP}$). The first body bias applied (BB1) has a smaller threshold voltage than with BB2. Measurements confirm that the threshold voltage of BB1 is detected at a lower voltage than BB2; this confirms the threshold voltage detector concept.

5.3 System Results

5.3.1 Ring Oscillator Load

A DC-DC converter and ring oscillator load is shown in Fig. 5.4. The DC-DC converter's SCN has a total fly capacitance of 200 pF and eight charge transfer switches. The converter uses two phase switching and a duty cycle of 50 %. Although not shown, the control circuitry is composed of drivers, a non-overlap clock generator, and level shifters. The DC-DC con-

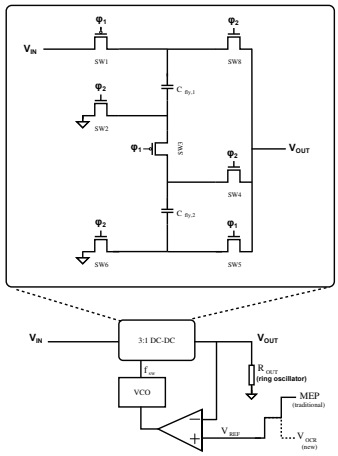


Figure 5.4. Test system with a series-parallel 3:1 DC-DC converter. V_{REF} was at the digital load's MEP for the traditional constraint and was set to V_{OCR} for the new constraint.

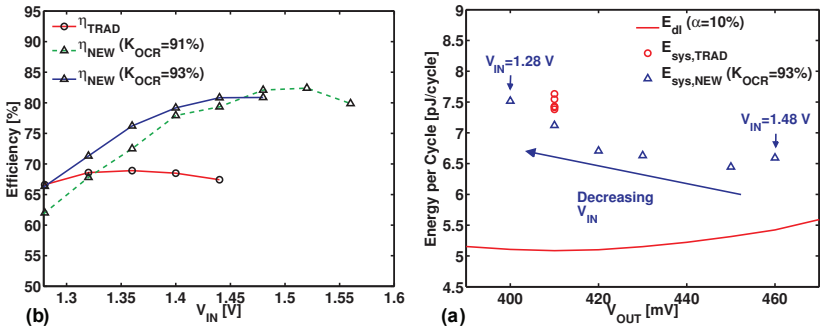


Figure 5.5. Effects of SIR and traditional regulation on (a) the efficiency of the DC-DC converter and (b) energy per cycle of the system.

verter can be configured for traditional regulation or with the (NEW) SIR technique. Traditional regulation is achieved by applying a fixed V_{OUT} to V_{REF}. SIR is achieved by connecting a voltage to V_{REF} that scales with V_{IN}.

The test system from Fig. 5.4 was simulated with V_{IN} from $\approx$ 1-1.55 V. The motivation for the input voltage is based on the prototype battery from [36]. The SIR technique results in a higher efficiency than the traditional regulation over most of this V_{IN} range. Additionally, the usable V_{IN} range with the SIR technique is larger. This characteristic is especially valid for when K_{OCR} is reduced. A lower K_{OCR} means lower load power at each V_{DD}, and thus, it is easier for the DC-DC converter to operate.

The effects of the DC-DC converter's efficiency on the (system) energy per cycle are shown in Fig. 5.5. The SIR technique scales V_{OUT} with V_{IN}

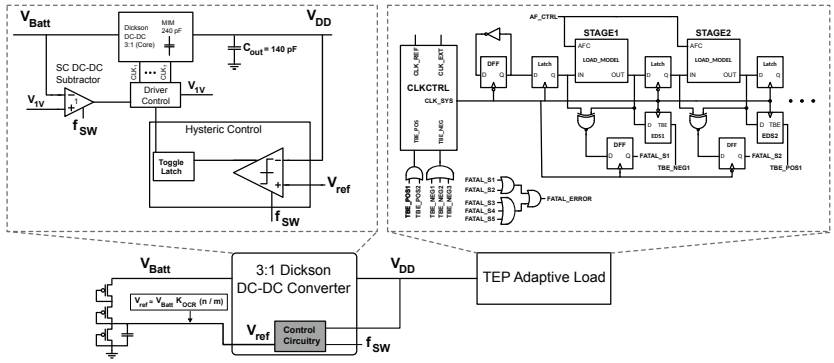


Figure 5.6. 3:1 DC-DC converter and TEP load schematic. ©2015 IEEE.

and gives lower energy per operation for most V_{IN} voltages. This behavior allows the converter to achieve close to η_{max} at each V_{IN}. The traditional regulation uses a fixed V_{REF}=410 mV, or the MEP of the ring oscillator. Using the SIR technique results in minimum energy savings of 8 % over the V_{IN} range [III]. Overall, the results of this system simulation show that by taking advantage of the digital load's energy profile (*i.e.* with SIR), energy savings can be achieved. As the energy per operation curves flatten with scaling (chapter 4), the SIR technique will become even more beneficial. In addition, as ultra-portable applications shift toward sub-5 μW load powers, the benefit of having reduced control circuitry (due to the SIR technique) will become more influential in improving efficiency at such low power levels.

5.3.2 TEP Load

To provide a more realistic load for the DC-DC converter, a 3:1 Dickson DC-DC converter was simulated with an adaptive TEP load in 28 nm FDSOI (Fig. 5.6). The DC-DC converter is the same that is used in section 3.2.2. However, a resistor divider was added to enable the SIR technique. The resistor divider generates a reference voltage for the feedback that is proportional to V_{Batt}. The load for the DC-DC converter is a TEP adaptive load. It includes a dual-phase latch pipeline with 5 stages, time borrow detection circuitry, and an adaptive clock generator. Additional details of the TEP adaptive load are found in [IX].

The simulation results of the DC-DC converter/TEP adaptive load system with local variations is shown in Fig. 5.7. The DC-DC converter uses the SIR technique to produce a V_{DD} = (V_{Batt}/3)*K_{OCR}, where K_{OCR} is 0.9. The average, best, and worst E_{cyc} of the DC-DC converter/TEP load sys-

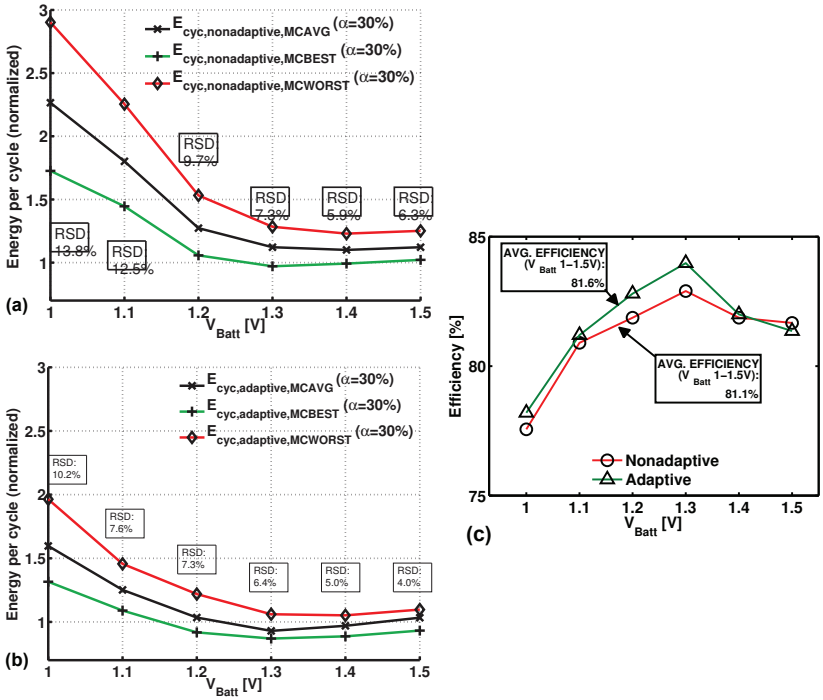


Figure 5.7. The average, best, and worst results from 10 Monte-Carlo runs on the DC-DC converter with (a) a TEP non-adaptive load (b) and an adaptive TEP load. Relative standard deviation (RSD) values are annotated in the boxes; (c) The DC-DC converter average efficiency of 10 Monte-Carlo iterations at each V_{Batt}.

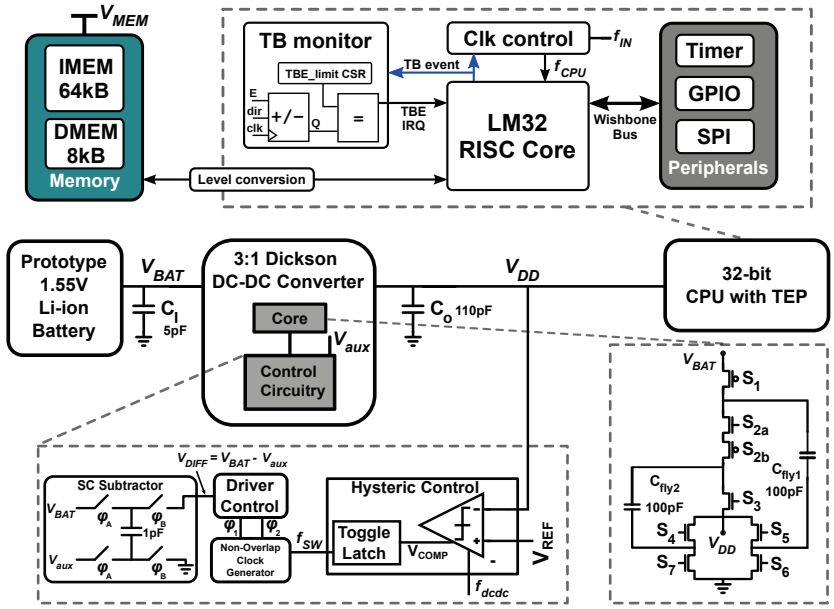


Figure 5.8. Schematic of the proposed battery/DC-DC converter/CPU system from [VIII]. ©2015 IEEE.

tem with Monte-Carlo iterations are shown. The comparison of Fig 5.7 (a) and 5.7 (b) not only shows that the average (system) energy per operation is less with the TEP adaptive load, but also that the deviation in the average energy per operation is reduced with the adaptive system.

The efficiency of the DC-DC conversion from the previous local variation simulation is shown in Fig. 5.7 (c). The DC-DC converter is able to maintain an efficiency over 78 % for V_{Batt}=1-1.5 V with the TEP adaptive load. We chose an α of 30 % as a worst case scenario for the DC-DC converter. At α = 30 %, the power would be the largest for the TEP adaptive load. The DC-DC converter was thus sized to meet the (average) power demand for the load at α = 30%. For α less than 30 % within the pipeline, the power at the load decreases, and the efficiency of the DC-DC converter is greater than or equal to the conversion efficiency at α=30%.

5.3.3 32-bit Processor with TEP

A prototype Li-ion battery, fully integrated switched-capacitor DC-DC converter, and CPU are proposed in Fig. 5.8. The main goal of the system is to operate at or near the CPU's minimum energy point despite changes in temperature or battery voltage. The 3:1 DC-DC converter steps down

the Li-ion battery voltage to near-threshold voltages. The battery has an improved (volumetric) energy density over traditional (nominal 3.6 V), a long cycle life, and spends most its discharge time with minimal voltage variation ($\approx$ 100 mV).

The prototype battery's characteristics allow for a more efficient DC-DC converter. The low nominal voltage increases the VCR (as compared to a traditional Li-ion battery). As a result, the DC-DC converter's SCN requires less charge transfer switches and capacitors, and can utilize thin-oxide transistors without breakdown issues. Besides the advantageous nominal voltage, the flat discharge curve of the battery allows for a single topology SC DC-DC converter to meet the output voltage requirements.

Achieving high energy efficiency in a battery/DC-DC converter/CPU system requires co-design. The energy profile of the CPU is the starting point of the co-design. This energy profile is constructed by simulating the current and maximum frequency at each V_{OUT}. The DC-DC converter needs to have a conversion ratio(s) that allows for efficient down-conversion from the battery voltage range to a target V_{OUT}. The target V_{OUT} is dependent on whether the CPU is throughput-constrained or energy-constrained. This thesis is mostly focused on energy constrained systems in which regulating at or slightly above the MEP is the main goal. For current technologies, the MEP is located near the threshold voltage.

The energy per cycle of digital logic can be defined as:

$$E_{DL} = P_{CPU} * T_{CLK}, \tag{5.1}$$

where P_{CPU} and T_{CLK} describe the power and clock period, respectively, of the CPU. The DC-DC converter's energy per cycle can also be described in terms of the T_{CLK}:

$$E_{DC-DC} = P_{DC-DC} * T_{CLK}. \tag{5.2}$$

Thus, combining (5.1) and (5.2), and recognizing that $P_{DC-DC} = P_{CPU} * ((1/\eta_{max}) - 1)$, gives the system energy per cycle:

$$E_{SYS} = E_{DL} + E_{DC-DC} = E_{DL} * (\frac{1}{\eta_{max}}). \tag{5.3}$$

For the desired (V_{OUT}) operation range, which is at or slightly above the MEP, the dynamic energy is dominant and thus $E_{DL} \approx C_{eff} V_{OUT}^2$. Rewrit-

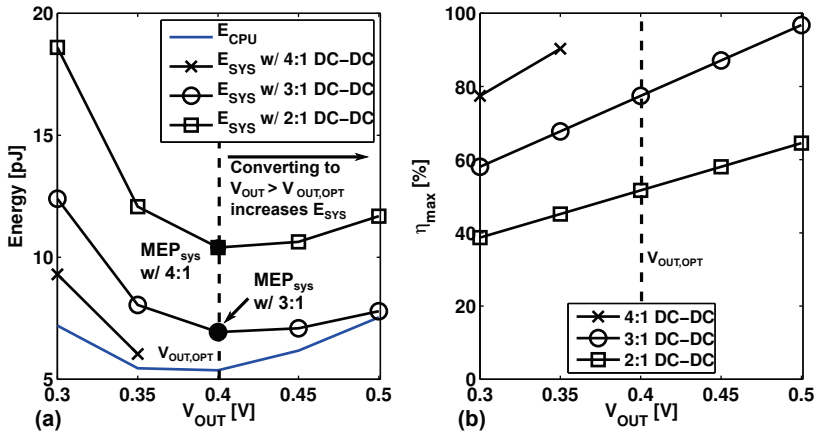


Figure 5.9. (a) Converting with higher efficiency to V_{OUT} > $V_{OUT,OPT}$ results in larger system energy consumption. (b) Resultant η_{max} for V_{IN}=1.55 V and multiple DC-DC topologies.

ing (5.3) based on this (E_{DL}) approximation gives:

$$E_{SYS} = C_{eff}V_{OUT}^2 * (\frac{1}{\eta_{max}}). \tag{5.4}$$

By expanding the η_{max} in terms of V_{OUT} then:

$$E_{SYS} = C_{eff}V_{OUT}^2(\frac{N * V_{IN}}{V_{OUT}}). \tag{5.5}$$

$$E_{SYS} = C_{eff}V_{OUT}(N * V_{IN}). \tag{5.6}$$

Equation (5.5) shows that the E_{DL} contribution ($C_{eff}V_{OUT}^2$) quadratically scales E_{SYS}, while the DC-DC contribution ($N * V_{IN}/V_{OUT}$) scales E_{SYS} linearly. Further simplification of Equation (5.6) shows that E_{SYS} increases linearly with V_{OUT}. In conclusion, regulating to a higher V_{OUT} in order to achieve higher efficiency in the DC-DC converter does not decrease the energy consumption.

The illustrate the previous conclusion, the measured energy per operation of a CPU E_{CPU} [VIII] and a DC-DC converter is calculated. Three different step-down topologies (*i.e.* 1/4, 1/3, 1/2), are used to explore a large range of V_{OUT} near the CPU's MEP as shown in Fig. 5.9 (a). Although the 1/3 and 1/2 topologies could both achieve higher efficiency at V_{OUT}>$V_{OUT,OPT}$ (see Fig. 5.9 (b)), the system energy MEP_{SYS} is at 0.4 V. This confirms the equations and conclusions above: increasing V_{OUT} above the $V_{OUT,OPT}$ in order to achieve higher efficiency in the DC-DC converter does not result in lower system energy consumption. However,

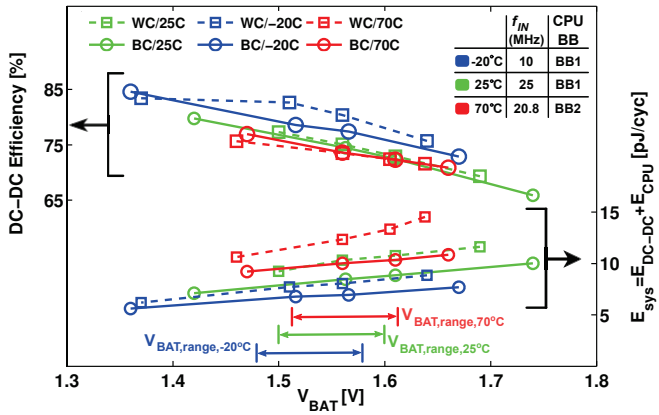


Figure 5.10. Measurement of the battery/DC-DC converter/CPU system.

for systems that do require operation at the MEP_{SYS}, it may be worthwhile to increase V_{OUT} to improve performance. Increasing from V_{OUT} to 0.4 V to 0.5 V would give a 240 % increase in performance (,*i.e.* 22.7 MHz to 77 MHz) and a 12.5 % increase in system energy.

For the battery/DC-DC converter/CPU system in Fig. 5.8, the main concern was energy consumption, and thus, the target was the MEP_{SYS}. We chose the 1/3 DC-DC converter topology that gave the highest efficiency near the MEP_{SYS} (5.9 (b)). The DC-DC converter and CPU shared the same input frequency (*i.e.* f_{dcdc}=f_{IN}) for all measurements. The CPU used the back-gate bias configuration of BB1 ($VBBP$=-0.5 V, $VBBN$=0 V) for high performance and BB2 ($VBBP$=0 V, $VBBN$=-0.5 V) for reduced leakage energy at high temperatures. Since the CPU operates only in active mode with power levels over 100 μW, the DC-DC converter losses are dominated by parasitic and conduction losses. These losses were minimized by using MIM fly capacitors and optimized transistor sizes according to [22], respectively. If the CPU would have had a sleep mode, RBB could have been used in the converter to reduce dominant control circuitry losses.

The measurement results of the battery/DC-DC converter/CPU system operating together are shown in Fig. 5.10. At temperatures ranging from -20 °C to 70 °C, and over 95 % of the battery discharge range, the average system energy consumption (Esys) was 8 pJ/cyc and the average DC-DC converter efficiency was 76.3 %. 8 pJ/cyc is considered state-of-the-art for a DC-DC converter/CPU system [VIII].

Since the previous measurements were done with traditional regulation (,*i.e.* DC-DC regulating to a fixed V_{OUT}), measurements were also per-

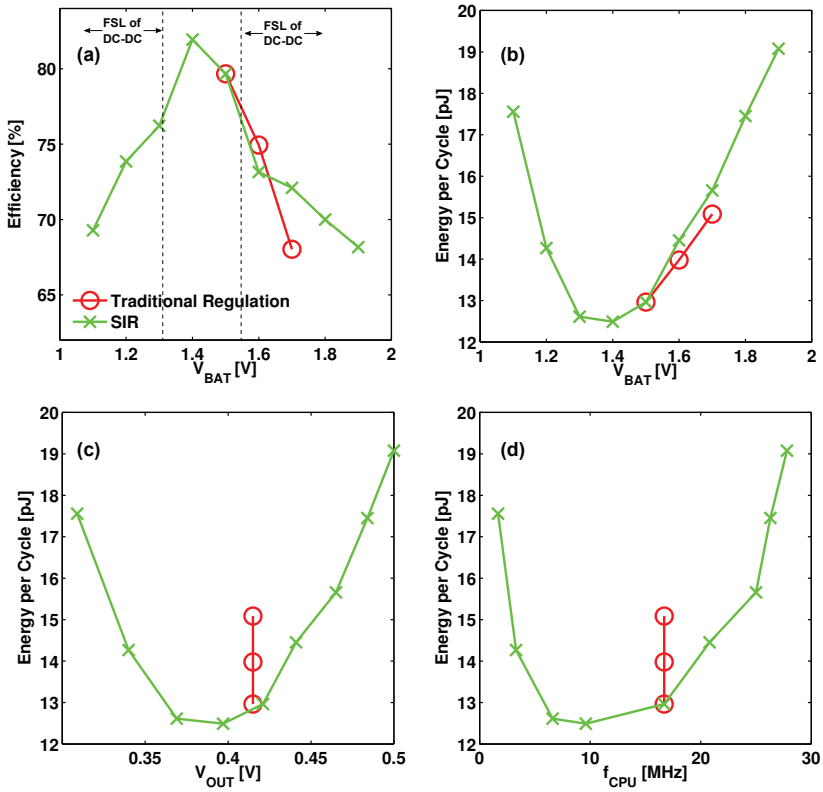


Figure 5.11. Measurements of the CPU with traditional and SIR. BB2 is applied in the CPU.

formed using the SIR technique as shown in Fig. 5.11. Using the SIR technique, the DC-DC converter provides good efficiency between 1.5 V and 1.6 V. Below 1.5 V, the lowered V_{DD} with SIR induces increases in power due to leakage. Above 1.6 V, the power raises due to switching. The increased power in each of these regions drives the DC-DC converter into FSL. Although the SIR technique did function with the CPU and did provide some advantages (*e.g.* large V_{BAT} range), the benefits in efficiency were limited due to the FSL operation. The FSL limitations were due to incorrect $P_{OUT,max}$ estimates (,*i.e.* 1.5 x higher), from the synthesis of the CPU.

5.4 Summary

The goal of this chapter was to identify the interdepedencies of the DC-DC converter and the ULE processor load. We examined how these blocks operate together and presented solutions to minimize the total system energy per operation. The SIR technique showed that system energy consumption could be reduced by exploiting the characteristics of the adaptive load. As process nodes scale and the load power decreases, the SIR technique will allow for further improvements in efficiency. A technique to identify the threshold voltage was also presented. This technique will be useful as a part of a future DC-DC/processor regulation system. Taking advantage of the prototype Li-ion battery characteristics also helped us in achieving state-of-the-art system energy consumption.

6. Conclusions

The goal of this thesis was to design DC-DC converters for ULE adaptive processor loads. The processors used an adaptive scheme called timing-error detection (TED). One of the processors is the first-known TED processor capable of sub-threshold operation. The main design constraints for the DC-DC converter were full integration and high efficiency. The thesis and the related scientific publications ([I]-[X]) presented challenges and solutions associated with achieving this goal.

Table 6.1 compares our three DC-DC converters to state-of-the-art SC DC-DC converters [14, 19, 21, 46] with similar power levels and NT output voltages. In general, our converters improved the state-of-the-art especially in terms of usable load range (with high efficiency), power density, and the use of practical input voltages (*i.e.* battery-connected). The DC-DC converter in [21] by Kwong *et al.* was the most similar reference to the converters in this thesis that the author could find. Kwong *et al.* used three topologies (1/3, 1/2, and 2/3) to step down from an input voltage of 1.2 V to NT voltages. They were able to achieve a large load power range (2-500 μW) due to scaleable switch widths. Using a single topology in our converters helped us in achieving higher efficiency down to much lower load power (*i.e.* nW). The DC-DC converter presented by Clerc *et al.* [46] was designed for slightly higher load power. It also took advantage of back-gate biasing in FD-SOI within its switches although details were limited. Our self-oscillating converter had a higher power density even assuming that the C_{OUT} in [46] was 0 pF (which was not reported). Bol *et al.* reported a DC-DC converter with high efficiency over a large power range in [14]. Unlike our proposed converters (which were also measured with processor loads), this converter required a large off-chip C_{OUT}. Additional DC-DC converters with NT output voltages such as [85, 86] were not considered in Table 6.1 since their power levels were much higher (5

x-10 x) than the target power levels of ultra-portable electronics (*i.e.* nW to μW).

Three conclusions were found from our implemented fully integrated DC-DC converters and adaptive loads. First, the ULE adaptive load characteristics should be considered when designing the DC-DC converter. Overall, ULE adaptive loads have relaxed constraints on ripple and regulation in terms of energy consumption and functionality. At NT voltages, the energy per operation flattens out relative to the supply voltage. As detailed in Publication III, taking advantage of this flatness with the SIR technique helps to reduce the system energy per operation. The measurements of ULE adaptive loads also showed that the functionality was insensitive to the supply voltage (from the DC-DC converter).

Second, as adaptive ULE load powers continue to reduce, the (increasingly dominant) control circuitry losses of the DC-DC converter need to be considered. Reducing the amount of control circuitry with a new topology (self-oscillating) and reducing the leakage energy within the control circuitry are both promising approaches. Due to its inherent ring oscillator, the self-oscillating converter was beneficial in reducing the amount of control circuitry components as detailed in chapter 3 and Publication VII. The self-oscillating converter achieved a peak efficiency of 87 % and was able to achieve efficiency over 75 % for 79 nW to 200 μW loads. Reducing leakage through back-gate biasing within the control circuitry also proved to be worthwhile in reducing losses within the Dickson DC-DC converter (see chapter 5 and Publication VIII). At V_{OUT}=0.465 V, the minimum efficiency of the Dickson DC-DC converter was 71% for 104 nW to 140 μW loads.

Third, exploring new energy sources is worthwhile for systems operating at NT. Regulating from a Li-ion (nominal 3.6 V) down to NT is challenging. The DC-DC converter by Wiechkowski *et al.* in [19], which achieved a peak efficiency of 56 %, is the only-known DC-DC converter with a Li-ion (3.6 V) input voltage and an NT output voltage. The challenges associated with stepping down from such a high input voltage stem primarily in avoiding breakdown voltages across switches and a small VCR. By using a prototype Li-ion battery with a low nominal voltage (1.55 V) and flat discharge profile, a single DC-DC converter topology can be used to convert to NT voltages at high efficiency. Additional details of this work are given in chapter 5 and Publication VIII.

Future SC DC-DC converters for ultra-portable electronics should focus on improving power density in order to drive down the costs of full integration. The power density needs to be improved to more closely match the power density of DC-DC converters with super-threshold loads (*e.g.* 3.2 W/mm^2 in [31]). The key elements in this effort needs to be on the fly capacitor and the overdrive voltage of the switches. Specifically, efforts should be made in identifying new methods to reducing voltage dependencies in MOSCAPs, evaluating new capacitor technologies (*e.g.* deep trench capacitors), and expanding on the back-gate biasing proposed in this work to increase overdrive voltages. As ultra-portable electronics continually push toward full-autonomy, increased functionality, improved security, high-efficiency and fully integrated DC-DC converters will become increasingly important.

Table 6.1. Comparison of the works presented here to state-of-the-art SC DC-DC converters.

	[46]	[14]	[21]	[19]	3:1 DC-DC (Section 3.1)	3:1 DC-DC (Section 3.2)	2:1 DC-DC (Section 3.3)
Technology	28nm UTBB FD-SOI	65nm CMOS	65nm CMOS	130nm CMOS	28nm CMOS	28nm UTBB FD-SOI (RVT)	28nm UTBB FD-SOI (LVT)
Topology	step-down SC	step-down SC	step-down SC	step-down SC/ LDO	step-down SC	step-down SC	self-oscillating step-down SC
C_{OUT}	N/R	3.3nF (off-chip)	0	0	200pF (MOM/MOS)	110pF	0pF
iVCR	1/3, 1/2	1/2	1/3, 1/2, 2/3	1/5	1/3	1/3	1/2
Tested Input / Output Voltage	1.1 / (0.33,0.45)	1-1.2V / (0.32 - 0.48V)	1.2V / (0.3 - 0.6V)	(2.5-3.6V) / (0.44V)	1-1.7V / (0.304-0.470V)	1-1.9V / (0.290-0.543V)	1-1.2V / (0.380 - 0.485V)
Load Range	130-5000µW[1]	5-320µW[1]	2-500µW[1]	100-350nW[1]	14µW-115µW	209nW-205µW	79nW-200µW
Load Range Min. Efficiency (η_{MIN})	N/R	η_{MIN}=75%	η_{MIN}=70%	η_{MIN}=30%	η_{MIN}=77%	η_{MIN}=71%	η_{MIN}=75%
Load Range in Ratio	1:39	1:64	1:250	1:125	1:8	1:981	1:2532
Efficiency max	75%@0.45V	81%@0.4V	78%@0.5V	56%@0.44V	[3]82%@0.350V	[4]81%@0.465V [4]76%@0.415V	[5]87%@0.46V
EEF_{max}	N/R	44%	47%	78%	[3]64%@0.350V	[4]65%@0.415V	[5]47%@0.460V
Efficiency (η) @ Sub-/Near-V_{th}	75%@0.45V	76%@0.4V	75%@0.5V	56%@0.4V	[3]75%@0.350V	[4]76%@0.415V	[5]75%@0.515V [5]77%@0.46V [5]77%@0.43V
Power Density @ η (mW/mm^2)	18.4@0.45V	[2]4.6@0.4V	2.05@0.5V	0.0006@0.4V	1.66@0.350V	5.5@0.415V	62@0.515V 19.2@0.46V 24@0.43V

[1]Estimated from paper [2]Does not include area of Cout [3]From simulations. [4]V_{BATT}=1.55V and NBB (GNDS=VDDS=0V) [5]V_{BATT}=1V and V_{BB}=1V
N/R: not reported

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Errata

Publication II

The contours in Fig. 3 (a) were incorrectly labeled as G_{ON}; they should have been labeled as transconductance (gm). Also, the (right) y-axis in Fig. 3 (b) was incorrectly labeled; the correct leakage scale is 10^{-11} to 10^{-4}.

There is an emerging class of energy-constrained adaptive processors that operate primarily at near-threshold voltages. Supplying the near-threshold voltage with high efficiency DC-DC converters is essential in realizing ultra-low energy consumption. The DC-DC converter should also be fully integrated to meet the increasingly small form factor requirements of modern ultra-portable electronics.

This work presents the implementation of three fully integrated switched-capacitor DC-DC converters and two fully integrated adaptive NT processors. By designing the DC-DC converter, elements of the adaptive processor load, and considering practical (battery) input voltages, the author is able to identify new system design methodologies and approaches that reduce energy consumption.

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